7.0inch RGB Display Module User Manual

Product Description

The product is a 7.0-inch RGB interface TFT LCD display module. The module supports the screen switching of 800x480 and 1024x600 resolutions, and supports up to 24bit rgb888 16.7M color display. There is no controller inside the module, so external controller is needed. For example, ssd1963 driver IC can be used as MCU LCD, and MCU with RGB controller (such as stm32f429, stm32ft767, stm32h743, etc.) can be used as RGB LCD. The module also has capacitive touch function and supports 5 touch points.

Product Features

- 7.0-inch color screen, support 24BIT RGB 16.7M color display, display rich colors
- Support 800x480 and 1024x600 resolution screen switching, the display effect is very clear
- Support 24 bit RGB parallel bus transmission
- Compatible with RGB interface connection of punctual atomic development board and wildfire development board
- Use capacitive touch screen to support 5 touch points
- Provides a rich sample program for STM32 platforms
- Military-grade process standards, long-term stable work
- Provide underlying driver technical support

Product Parameters

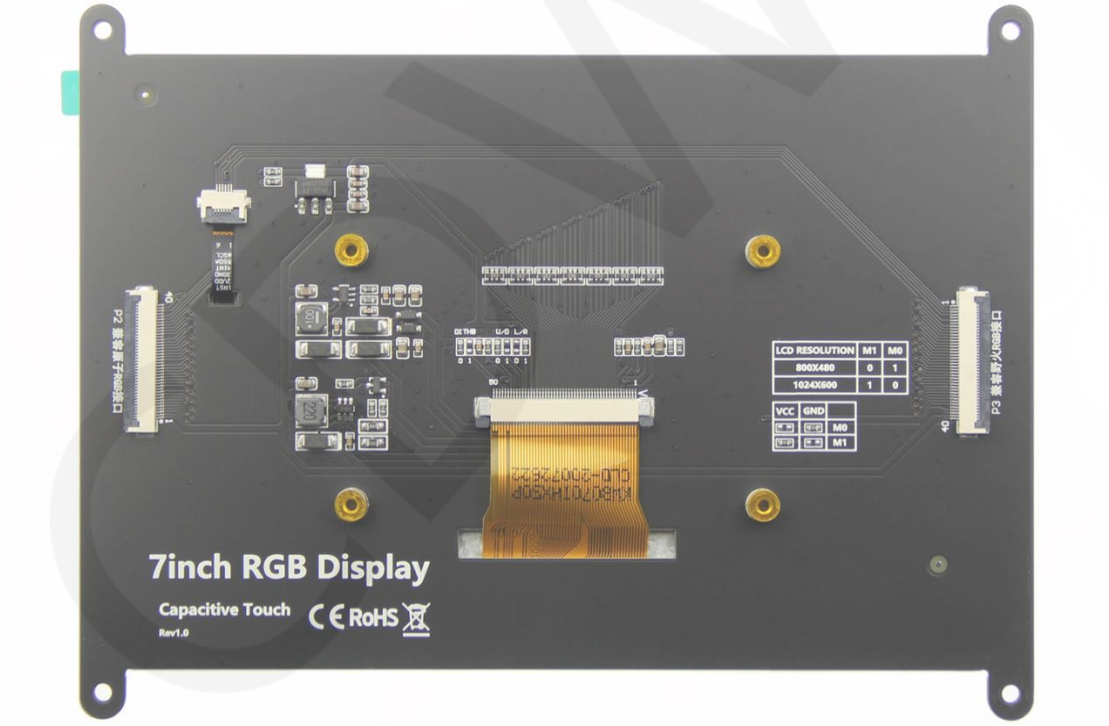
Name	Description
Display Color	RGB888 16.7M (compatible with rgb5665k) color
SKU	800x480:MRG7101(no touch), MRG7111(have touch) 1024x600:MRG7102(no touch),MRG7122(have touch)
Screen Size	7.0(inch)
Type	TFT
Driver IC	None

Resolution	800*480 or 1024x600 (Pixel)
Module Interface	24Bit RGB parallel interface
Touch Screen Type	Capacitive touch screen
Touch IC	FT5426
Active Area	800x480: 153.84x85.63(mm) 1024x600: 154.21x85.92(mm)
Module PCB Size	164.90x124.27(mm)
Operating Temperature	-10℃~60℃
Storage Temperature	-20℃~70℃
Input Voltage	5V
IO Voltage	3.3V
Power Consumption	800x480: 67mA(The backlight is off), 467mA(The backlight is the brightest) 1024x600: 104mA(The backlight is off), 310mA(The backlight is the brightest)
Product Weight(Net weight)	236g

Interface Description

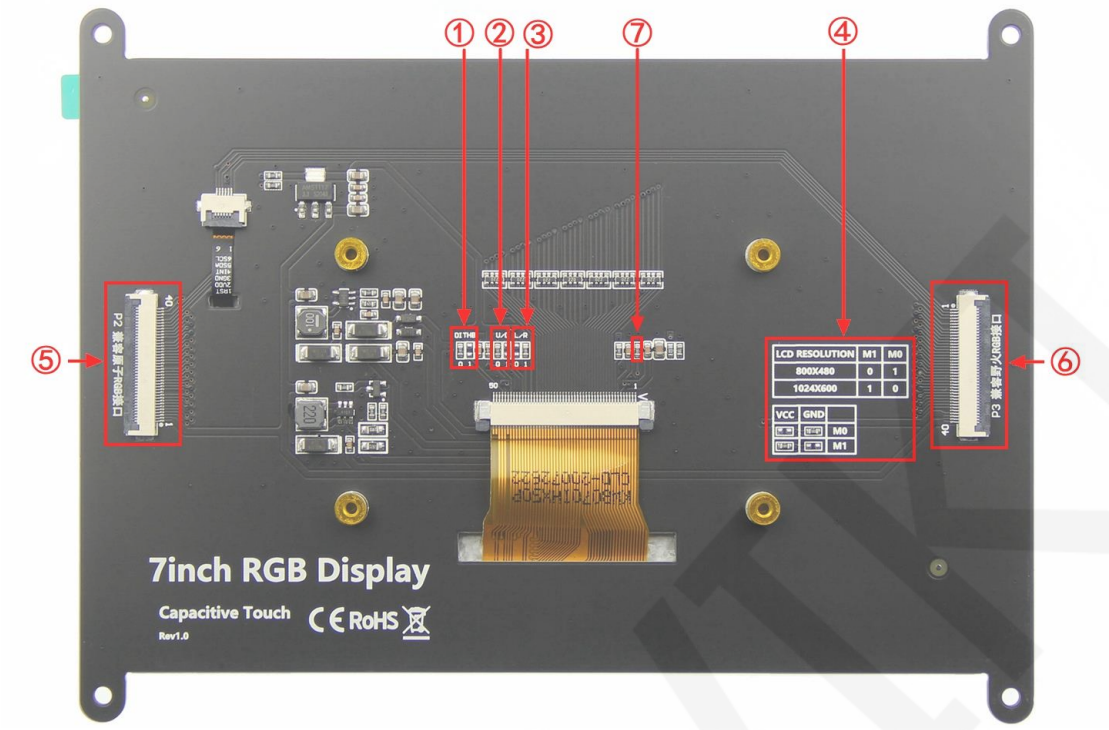
The module is compatible with the RGB interface of punctual atomic development board and wildfire development board, and is connected with the development board through 40 pin flexible cable. The appearance is shown in Picture 1 and Picture 2.

Picture1. Front view of module



Picture2. Back view of module

The module interface and selection circuit are shown in Picture 3:



Picture3. The module interface and selection circuit

Each identification circuit in Picture 3 is described as follows:

①--DITHB selection circuit
②--U/D selection circuit
③--L/R selection circuit
④--Screen resolution selection circuit
⑤--P2 interface (compatible with atomic RGB interface)
⑥--P3 interface (compatible with wildfire RGB interface)
⑦-- B7 Data line pull resistance (required to define module ID, applicable to atomic program)

1. Screen internal Dithering display function settings

   Weld the 0 position resistance of DITHB and disconnect the 1 position resistance to enable the internal Dithering display function of the display panel;

   Weld the 1 position resistance of DITHB, disconnect the 0 position resistance, and turn off the internal Dithering display function of the screen;

   Default welding 0 position resistance, disconnect 1 position resistance

2. Screen display up and down flip settings

Weld the resistance at position 0 of U / D, disconnect the resistance at position 1, and the screen will turn down;

Weld the resistance at position 1 of U / D, disconnect the resistance at position 0, and the screen will turn upward;

Default welding 0 position resistance, disconnect 1 position resistance

3. Screen display left and right flip settings

weld the resistance at position 0 of L / R, disconnect the resistance at position 1, and the screen will turn to the left;

Weld the resistance at position 1 of L / R, disconnect the resistance at position 0, and the screen will turn right;

Default welding 1 position resistance, disconnect 0 position resistance

4. Screen resolution selection

As shown in the screen resolution selection circuit, the module supports screen switching of 800x480 and 1024x600 resolutions.

Weld M0 resistance to GND, M1 resistance to VCC, select 1024x600 resolution;

Weld M0 resistance to VCC, M1 resistance to GND, and select 800x480 resolution;

5. Precautions for connecting to wildfire development board

If connected to wildfire i When using the MX6ULL ARM Linux development board, it is necessary to remove the pull resistance on the B7 data line referred to by label 7 and the M0 and M1 resistance referred to by label 4, otherwise the development board will not run

6. P2 and P3 interface pins are described as follows:

P2 interface (compatible with atomic RGB interface) pin description		
Number	**Pin name**	**Pin description**
1	**VCC5**	Power input pin（connect to 5V）
2	**VCC5**	Power input pin（connect to 5V）
3~10	**R0 ~ R7**	8-bit RED data pin

11	GND	power ground pin
12~19	G0 ~ G7	8-bit GREEN data pin
20	GND	power ground pin
21~28	B0 ~ B7	8-bit BLUE data pin
29	GND	power ground pin
30	PCLK	Pixel clock control pin
31	HSYNC	Horizontal synchronous signal control pin
32	VSYNC	Vertical synchronous signal control pin
33	DE	Data enable signal control pin
34	BL	LCD backlight control pin
35	TP_CS	Capacitor touch screen reset pin (resistance touch screen chip selection pin)
36	TP_MOSI	Data pin of IIC bus of capacitance touch screen (write data pin of SPI bus of resistance touch screen)
37	TP_MISO	Resistance touch screen SPI bus read data pin (capacitance touch screen not used)
38	TP_CLK	IIC bus clock control pin of capacitive touch screen (SPI bus clock control pin of resistance touch screen)
39	TP_PEN	Touch screen interrupt control pin
40	RST	LCD reset control pin (effective at low level)

Pin description of P3 interface (compatible with wildfire RGB interface)

Number	Pin name	Pin description
1	TP_SCL	IIC bus clock control pin of capacitive touch
2	TP_SDA	Data pin of IIC bus of capacitance touch screen
3	TP_PEN	Touch screen interrupt control pin
4	TP_RST	Capacitor touch screen reset pin
5	GND	power ground pin
6	BL	LCD backlight control pin
7	DISP	LCD display enable pin (not used)
8	DE	Data enable signal control pin

9	**HSYNC**	Horizontal synchronous signal control pin
10	**VSYNC**	Vertical synchronous signal control pin
11	**PCLK**	Pixel clock control pin
12~19	**B7 ~ B0**	8-bit BLUE data pin
20~27	**G7 ~ G0**	8-bit GREEN data pin
28~35	**R7 ~ R0**	8-bit RED data pin
36	**GND**	power ground pin
37	**VCC3.3**	Power input pin（connect to 3.3V）
38	**VCC3.3**	Power input pin（connect to 3.3V）
39	**VCC5**	Power input pin（connect to 5V）
40	**VCC5**	Power input pin（connect to 5V）

Hardware Configuration

The hardware circuit of the LCD module consists of nine parts: voltage stabilizing circuit, backlight control circuit, screen resolution selection circuit, 50pin display interface, drain circuit, P2 user interface, P3 user interface, capacitive touch screen interface circuit and power supply circuit.

1. The voltage stabilizing circuit is used to provide VGH, VGL and VCOM voltage to the display screen, so as to ensure the stability of the display screen.
2. The backlight control circuit is used to provide backlight voltage to display screen and adjust backlight brightness.
3. The screen resolution selection circuit is used to select the display type (distinguished according to the resolution). Its principle is to connect pull-up or pull-down resistors on R7, G7 and B7 data lines respectively, and then determine the resolution of the display screen used by reading the status of the three data lines (equivalent to reading the display screen ID), so as to select different configurations. In this way, a test example can be compatible with multiple displays in software.
4. The 50pin display interface is used to access and control the display screen.
5. The drain circuit is used to balance the data line impedance between the display and the user interface.

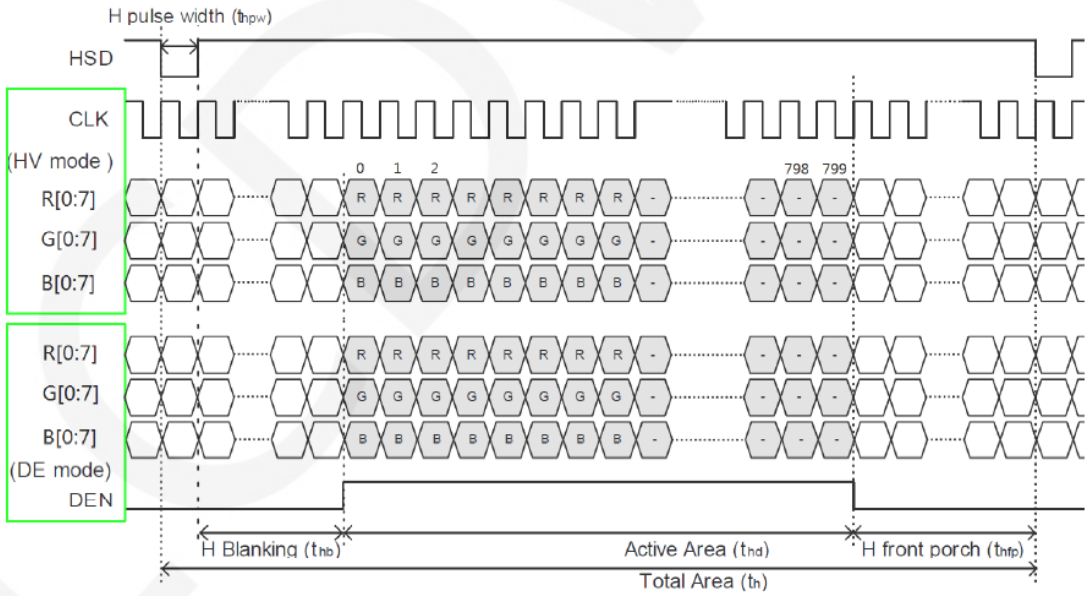
6. P2, P3 user interface is used for external development board.
7. Capacitive touch screen interface circuit is used to intervene capacitive touch screen and control IIC pin pull-up.
8. The power circuit is used to convert the input 5V power supply to 3.3V.

working principle

1. Introduction to RGB LCD

High resolution and large size display screen generally does not have MCU screen interface, all adopt RGB interface, which is RGB LCD. This LCD has no built-in control IC and no built-in video memory, so it needs external controller and video memory.

The general RGB LCD has 24 color data lines (R, G, B each 8) and De, vs, HS, PCLK four control lines. It is driven by RGB mode, which generally has two driving modes: de mode and HV mode. In de mode, de signal is used to determine valid data (when De is high / low, data is valid), while in HV mode, row synchronization and field synchronization are required to represent the rows and columns of scanning. The row scan sequence diagram of de mode and HV mode is shown in the following figure:



It can be seen from the figure that the time sequence of de mode and HV mode is basically the same. De signal (DEN) is required for den mode, while de signal is not required for HV mode. The HSD in the figure is the HS signal, which is used for line

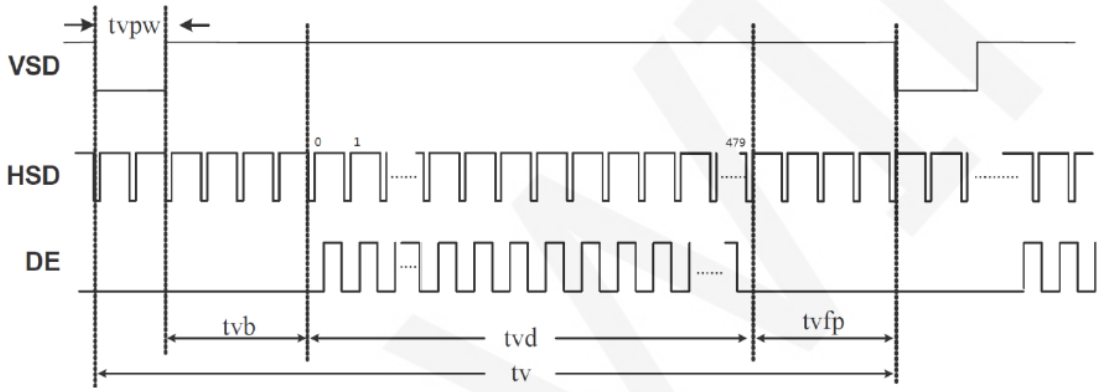
synchronization. Note: in de mode, the HS signal can not be used, that is, the LCD can still work normally without receiving the HS signal.

thpw is the effective signal pulse width of horizontal synchronization, which is used to indicate the beginning of a line of data;

thb is the horizontal back corridor, which represents the number of pixel clocks from the horizontal effective signal to the effective data output;

thfp is the horizontal front corridor, which indicates the number of pixel clocks from the end of a row of data to the beginning of the next horizontal synchronization signal.

The vertical scanning sequence diagram is as follows:



VSD is vertical synchronous signal;

HSD is the horizontal synchronous signal;

DE is data enable signal;

tvpw is the effective signal width of vertical synchronization, which is used to indicate the beginning of a frame of data;

tvb is the vertical rear corridor, which represents the number of invalid lines after the vertical synchronization signal;

tvfp is a vertical front corridor, which indicates the number of invalid lines after the end of one frame data output and before the start of the next vertical synchronization signal;

As can be seen from the figure, a vertical scan is exactly 480 effective De pulse signals. Each de clock cycle scans one line, and a total of 480 lines are scanned to complete the display of a frame of data. This is the scan sequence of 800 * 480 LCD panel. The timing of other resolution LCD panels is similar.

Instructions for use

1. STM32 instructions

Wiring instructions:

See the interface description for pin assignments.

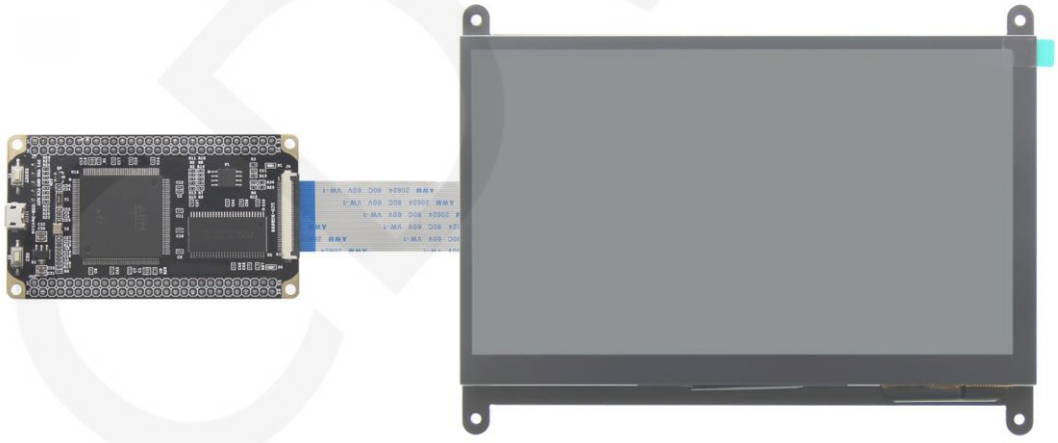
Wiring is carried out in two steps:

A. Use 40pin flexible cable to connect the RGB interface on the display module. Among them, P2 interface is compatible with punctual atomic development board, and P3 interface is compatible with wildfire development board (as shown in Picture 4, the connection method of P3 interface is the same as that of P2 interface).

Picture 4. Connect RGB display module

B. After the display module is connected successfully, connect the other end of the flexible cable to the development board (as shown in Picture 5 and Picture 6). It should be noted that the flat cable should not be inserted reversely, so that the 1 ~ 40 pins of the display module interface and the 1 ~ 40 pins of the development board interface should be connected one by one.

Picture 5. Connect atomic core development board



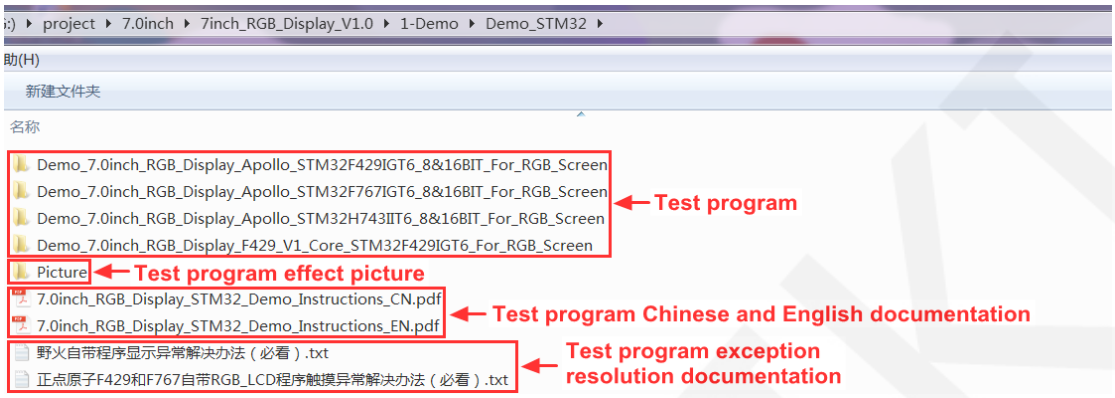
Picture 6. Connect wildfire core development board

Operating Steps：

A. Connect the LCD module and the STM32 MCU according to the above wiring instructions, and power on;

B. Select the STM32 test program to be tested, as shown below:

(Test program description please refer to the test program description document in the test package)



C. Open the selected test program project, compile and download;

detailed description of the STM32 test program compilation and download can be found in the following document:

http://www.lcdwiki.com/res/PublicFile/STM32_Keil_Use_Illustration_EN.pdf

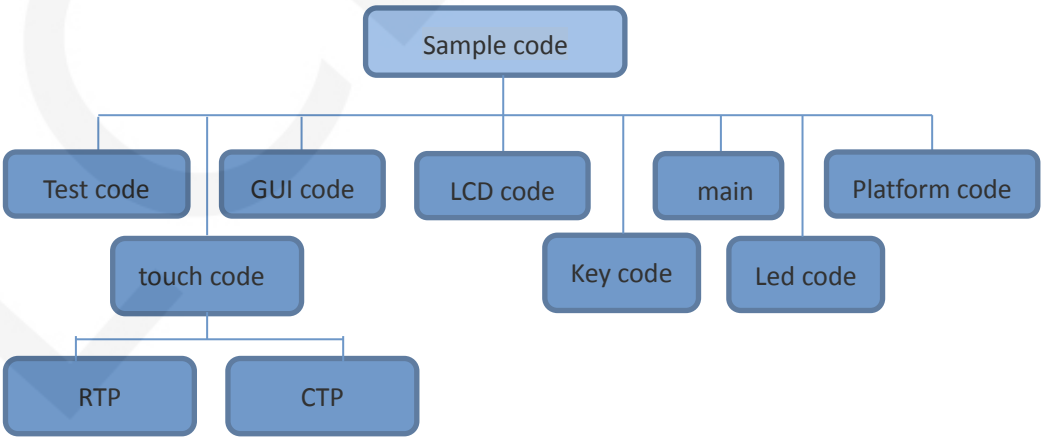
D. If the LCD module displays characters and graphics normally, the program runs successfully;

Software Description

1. Code Architecture

A. STM32 code architecture description

The code architecture is shown below:



The Demo API code for the main program runtime is included in the test code;

LCD initialization and related bin parallel port write data operations are included in the LCD code, Including MCD LCD and RGB LCD;

Drawing points, lines, graphics, and Chinese and English character display related operations are included in the GUI code;

The main function implements the application to run;

Platform code varies by platform;

Touch screen related operations are included in the touch code;

The key processing related code is included in the key code;

The code related to the led configuration operation is included in the led code;

Common software

This set of test examples requires the display of Chinese and English, symbols and pictures, so the modulo software is used. There are two types of modulo software: Image2Lcd and PCtoLCD2002. Here is only the setting of the modulo software for the test program.

The **PCtoLCD2002** modulo software settings are as follows:

Dot matrix format select Dark code

the modulo mode select the progressive mode

Take the model to choose the direction (high position first)

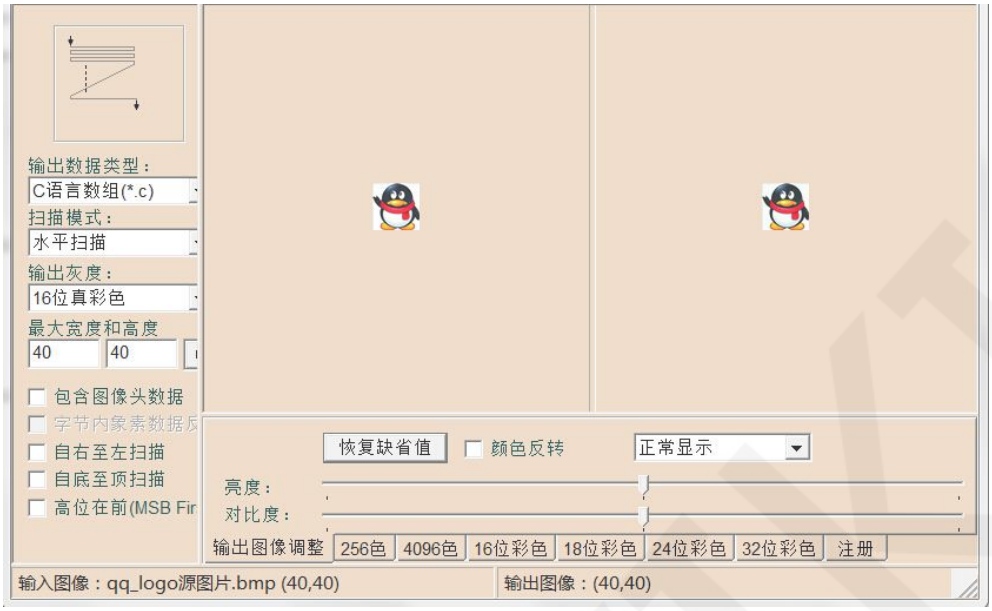
Output number system selects hexadecimal number

Custom format selection C51 format

The specific setting method is as follows:

http://www.lcdwiki.com/Chinese_and_English_display_modulo_settings

Image2Lcd modulo software settings are shown below:



The Image2Lcd software needs to be set to horizontal, left to right, top to bottom, and low position to the front scan mode.