FT5x26

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5x26 Series ICs are the single-chip capacitive touch panel controller with Cortex M0 core for supporting large-sized mutual capacitive touch panel. FT5x26 adopts the mutual capacitance and full screen common mode scan technology, and support true multi-touch capability, ideal for up to 15.6 " panel applications performance. Being coupled with a mutual capacitive touch panel, FT5x26 can implement the user-friendly inputting function and be widely used in various portable devices in large size, such as Ultrabooks, PADs, MIDs and GPS, etc.
As FT5x26 is in a same series, this datasheet will present them together and list differences among them individually in the following sections.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- ARM Cortex M0 core MCU
- True Multi-Touch with up to 10 Points of Absolute X and Y Coordinates
- Enhanced Immunity to RF and power Interferences
- Auto Calibration and Compensation for Environmental Variations
- FT5x26 Supports up to 48 TX lines + 72 RX lines
- Fully Programmable Scan Sequences to Support Various TX/RX Configurations
- High Report Rate: Up to 100Hz
- Capable of Driving Single Channel Resistance up to 10KΩ (including both TX and RX lines)
- Capable of Driving Single Channel Capacitance up to 120 pF (including both TX and RX lines)
- Optimal Sensing Mutual Capacitor for each node 1pF~4pF
- Touch Resolution up to 100 Dots per Inch (dpi) or above -- depending on the Panel Size
- 12-Bit ADC Accuracy
- Optional Interfaces : I^2C/SPI/USB
- 2.8V to 3.6V Operating Voltage
- IOVCC Supports from 1.8V to 3.6V
- Built-in LDO for Digital Circuits
- Support Win8
- Supports up to 15.6" Touch Screen
- 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Hibernate Mode
- Operating Temperature Range: -20℃ to +85℃
- Package, BGA 160 ball, 5x10x0.6mm, pitch 0.5mm

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5x26 accommodate a wide range of applications, some typical examples are listed below.

- Ultrabook
- PAD
- Electronic Book
- MID
- GPS

FT5x26 support large Touch Panel, users may find out their target IC from the following table.

Model Name	Panel		Package			Touch Panel Size
	TX	RX	Type	Pin	Size	
FT5826QSL	36	48	BGA	160	10x5x0.6mm	≤10.1"
FT5926QSM	40	58	BGA	160	10x5x0.6mm	≤12.5"
FT5B26QSN	44	66	BGA	160	10x5x0.6mm	≤14.1"
FT5C26QSP	48	72	BGA	160	10x5x0.6mm	≤15.6"

Remarks: The large TP size is supported for Win8.

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5x26.

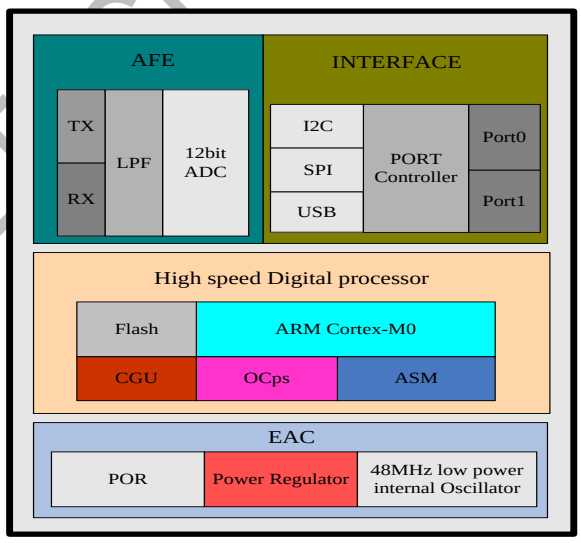


Figure 2-1 FT5x26 System Architecture Diagram

The FT5x26 is comprised of five main functional parts which are listed as below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- ARM Cortex M0 core MCU

For ARM Cortex M0 core MCU, larger program and data memories are supported.
Complex signal processing algorithms are implemented with firmware running on MCU and signal process unit to detect the touches reliably and efficiently. Communication protocol driver is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C/SPI/USB: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - /RST: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.

2.2 Power Supply Selection

There are two options for power supply of FT5x26, and it is selected by PSEL pin .

- When PSEL=0, FT5x26 is powered by external Power supply, the voltage is 2.8V~3.6V, connect to VDD3 and VDDA , VBUS is connected to VDD3
- When PSEL=5V(VBUS), FT5x26 is powered by USB, the voltage is 4.5V~5.5V, connect to VBUS, VDD3 is around 3V, VDDA is Connected to VDD3.

A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply.

IOVCC is 1.8~3.6V for Digital I/O.

VDDD and VDD5 are provided by internal circuit.

A decoupling capacitor(1uF) must be placed between each power pin and ground.

2.3 MCU

This section describes some critical features and operations supported by the ARM Cortex-M0 core MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- Program Memory: 48KB Flash
- Data Memory: 48KB SRAM
- Timer: A number of timers are available to generate different clocks
- Master Clock: 24/ 48MHz from a 48MHz RC Oscillator or external crystal and PLL
- Clock Manager: To control various clocks under different operation conditions of the system

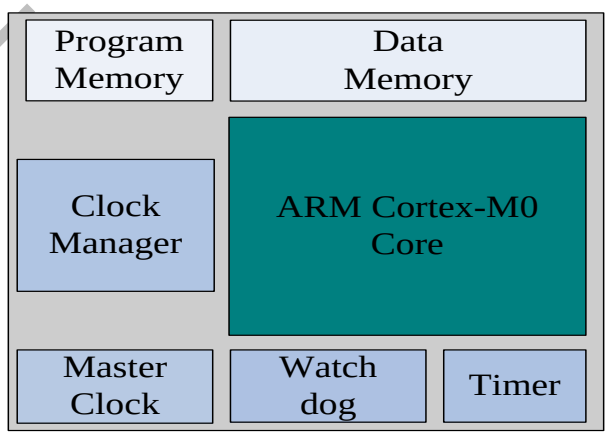


Figure 2-2 MCU Block Diagram

2.4 Operation Modes

FT5x26 operates for the Win8 spec or in the following three modes:

- Active Mode

When in this mode, FT5x26 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5x26 to speed up or to slow down.

- Monitor Mode

When in this mode, FT5x26 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5x26 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- Hibernate Mode

In this mode, the chip is set in power down mode. It shall only respond to the "RESET" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.5 Host Interface

Figure 2-3 shows the interface between a host processor and FT5x26. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5x26 to the Host
- Reset Signal from the Host to FT5x26

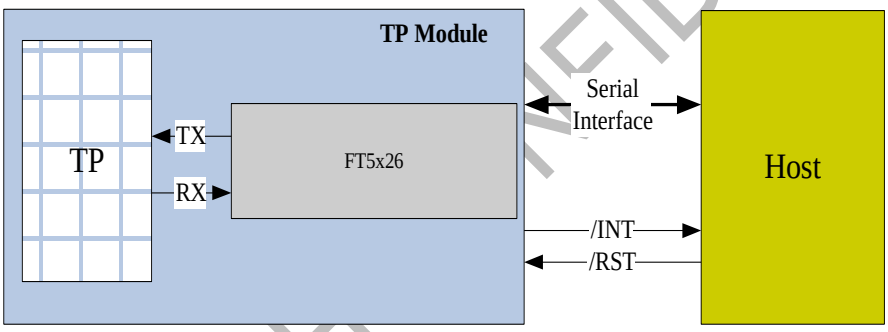


Figure 2-3 Host Interface Diagram

The serial interfaces is I2C or SPI. The details of this interface are described in detail in Section **2.6**. The interrupt signal (/INT) is used for FT5x26 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to reset FT5x26. After resetting, FT5x26 shall enter the Active mode.

2.6 Serial Interface

FT5x26 supports the I2C , SPI or USB interfaces, which can be used by a host processor or other devices.

2.6.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

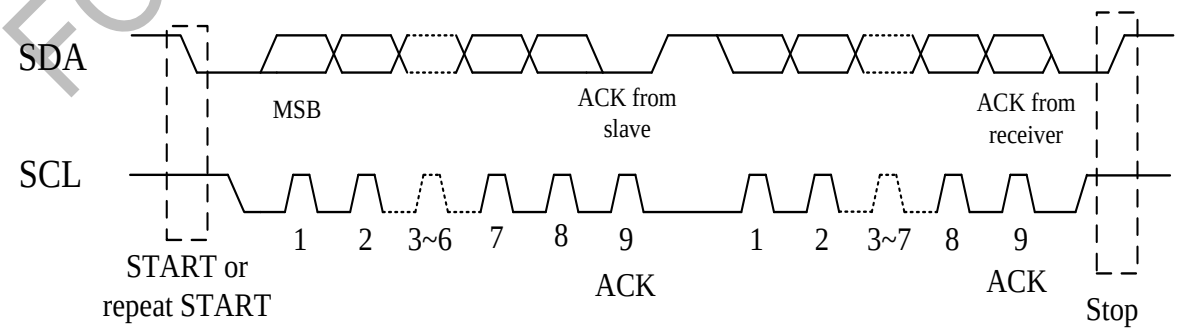


Figure 2-4 I2C Serial Data Transfer Format

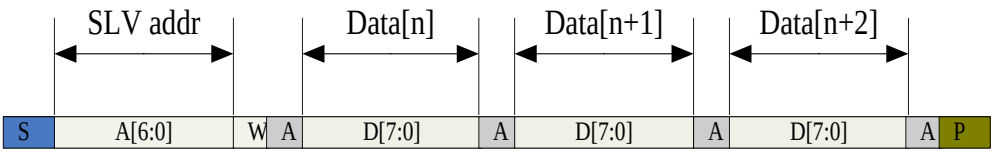


Figure 2-5 I2C master write, slave read

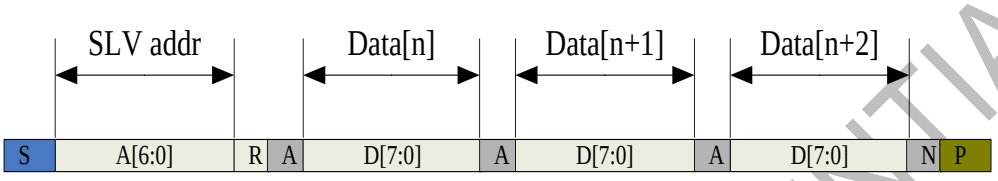


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the symbols used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

2.6.2 SPI

SPI is a 4 wire serial interface. The following is a list of the 4 wires:

- SCK: serial data clock
- MOSI: data line from master to slave
- MISO: data line from slave to master
- SLVSEL: active low select signal

SPI transfers data at 8bit packets. The phase relationship between the data and the clock can be defined by the two registers: phase and pole. Some data transfer examples can be found in Figure 2-7 to Figure 2-10.

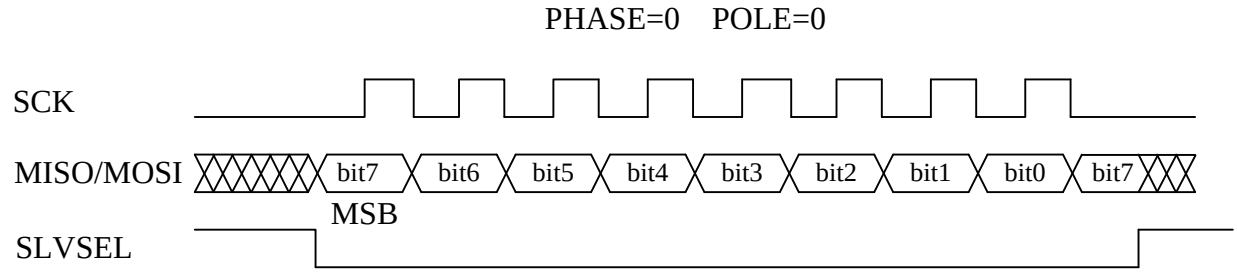


Figure 2-7 SPI Data Transfer Format (Phase=0, POLCK=0)

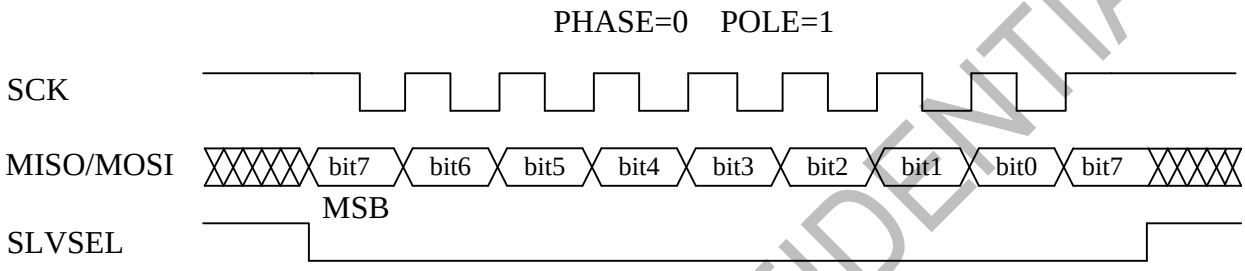


Figure 2-8 SPI Data Transfer Format (PHASE=0, POLCK=1)

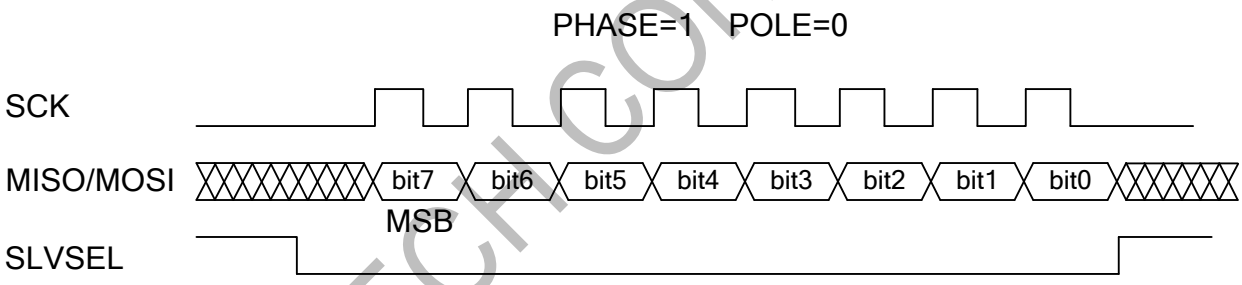


Figure 2-9 SPI Data Transfer Format (Phase=1, POLCK=0)

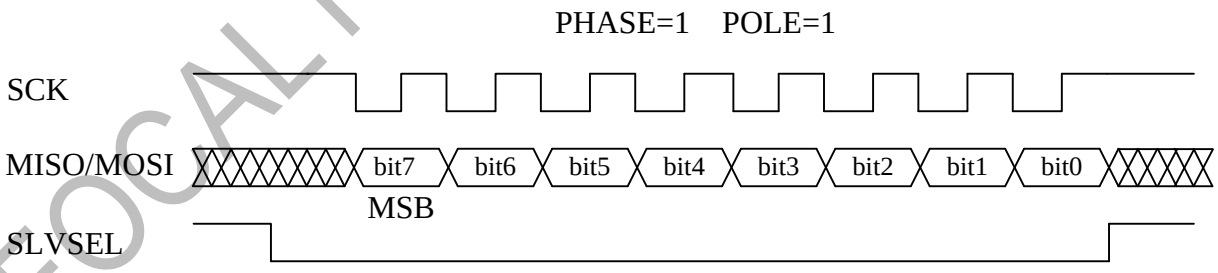


Figure 2-10 SPI Data Transfer Format (Phase=1, POLCK=1)

SPI can be configured into either Master or Slave mode via firmware. When in the Master mode, the SPI needs to supply the data clock, whose frequency relationship with the Master clock can be set by firmware. When it is configured in the Slave mode, the clock, SCK, is supplied by the external Master. The maximum data clock frequency must not be higher than $\frac{F_{mclk}}{8}$.

SPI Interface Timing Characteristics is shown in the following Figure2-11,Figure2-12, Figure2-13, Figure2-14 and Table 2-3.

PHASE=0

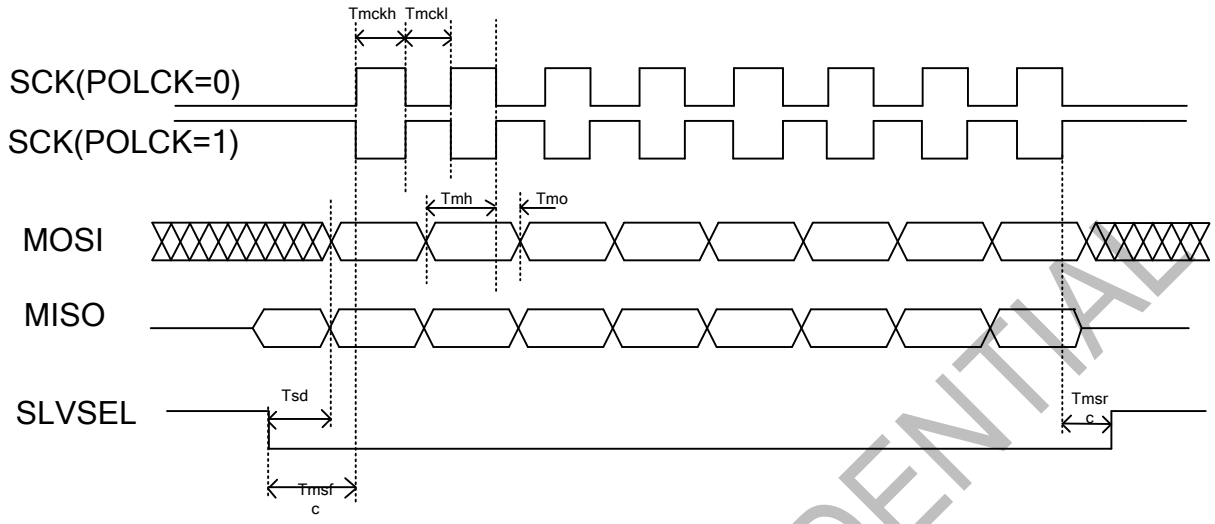


Figure 2-11 SPI master Timing PHASE =0

PHASE=1

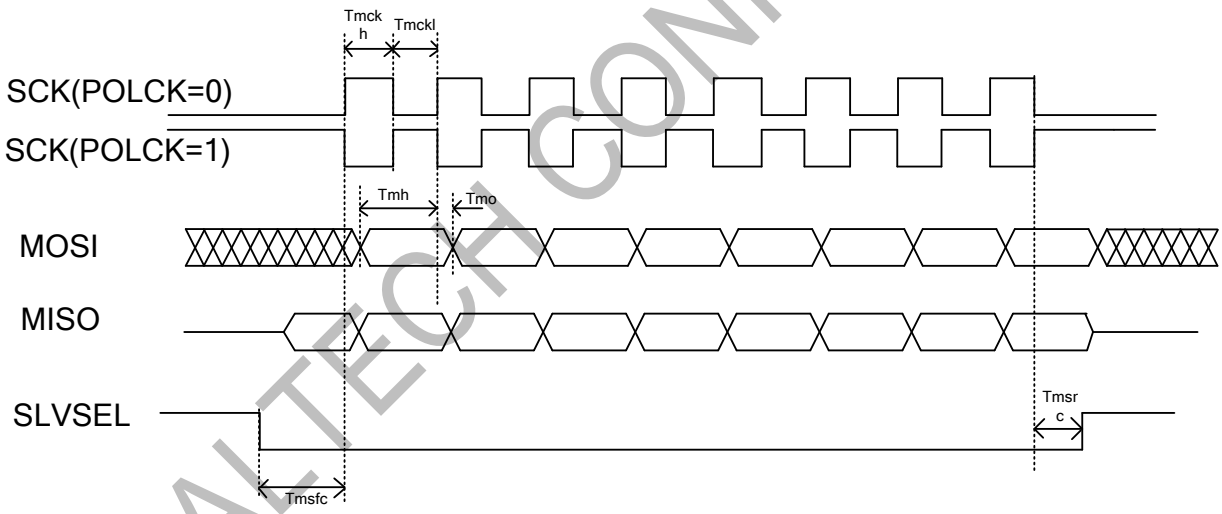


Figure 2-12 SPI master Timing PHASE =1

PHASE=0

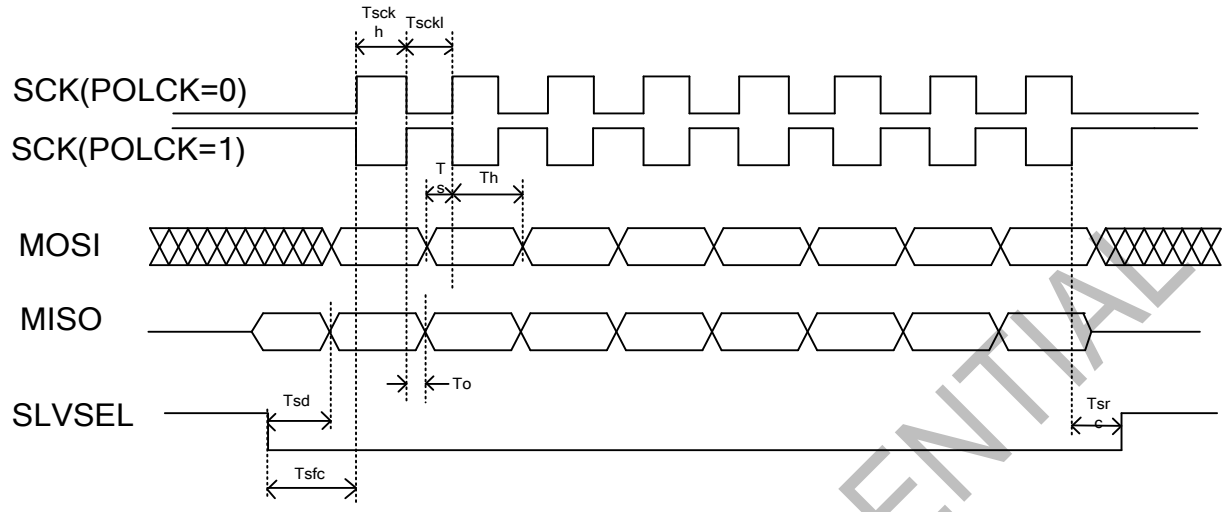


Figure 2-13 SPI slave Timing PHASE = 0

PHASE=1

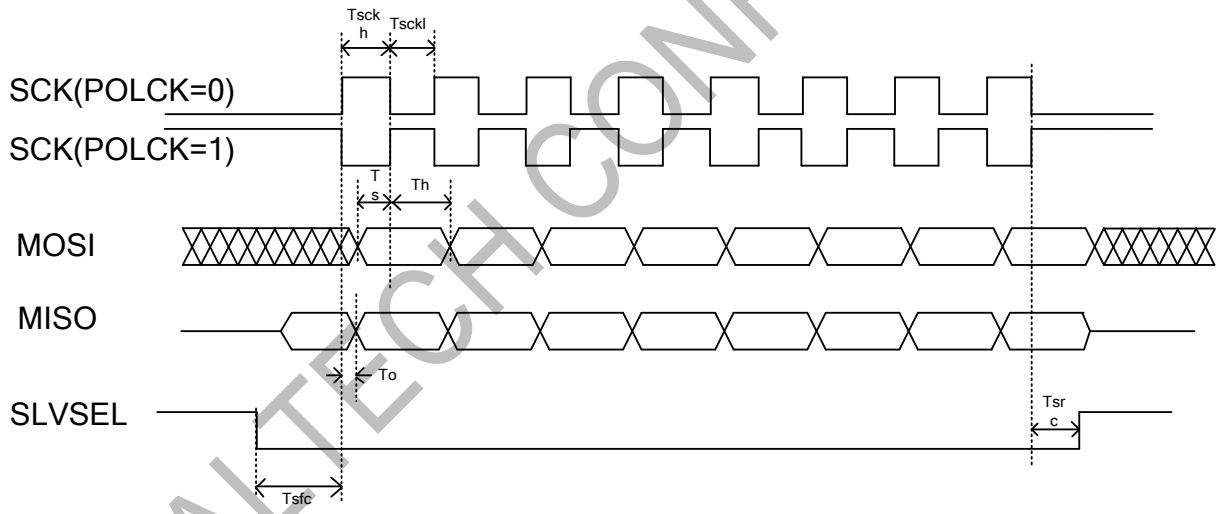


Figure 2-14 SPI slave Timing PHASE = 1

Table 2-3 SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode timing (see figure 2-11,2-12)				
Tmckh	sck high time	4×Tsysclk	--	ns
Tmckl	sck low time	4×Tsysclk	--	ns
Tmo	sck shift edge to mosi data change	0	--	ns
Tmh	mosi data valid to sck shift edge	3×Tsysclk	--	ns
Tsd	slvsel falling edge to mosi data valid	4×Tsysclk	--	ns
Tmsfc	slvsel falling edge to first sck edge	(Tmckh+Tmckl)/2	--	ns
Tmsrc	last sck edge to slvsel rising edge	(Tmckh+Tmckl)/2	--	ns

Slave mode timing(See figure 2-13,2-14)				
Tsckh	sck high Time	4×Tsysclk	--	ns
Tsckl	sck low Time	4×Tsysclk	--	ns
Tsd	slvsel falling edge to Miso valid data time	0	4xTsysclk	ns
Ts	Mosi Data valid to sck sample edge	0	--	ns
Th	sck sample edge to Mosi data change	4×Tsysclk	--	ns
To	sck shift edge to Miso data change	0	4xTsysclk	ns
Tsfc	slvsel falling edge to first sck edge	4×Tsysclk	--	ns
Tsrc	last sck edge to slvsel rising edge	4×Tsysclk	--	ns
*Tsysclk is equal to one period of the device system clock				

2.6.3 USB

USB is configured in device mode, and a Full speed USB function is supported. The USB function controller is as follows.

- USB 2.01-compliant composite device , full speed (12Mbps) ;
- Require external crystal (12MHz) ;
- Support USB LPM L1;
- integrated transceiver;
- Support USB-HID protocol for Win8.
- Vendor ID: 0x2808

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Note	Unit
Power Supply Voltage 1	VDDA - VSSA	-0.3 ~ +3.6	1, 2	V
Power Supply Voltage 2	VDD3 – VSS	-0.3 ~ +3.6	1, 3	V
I/O Digital Voltage	IOVCC	1.8~3.6	1	V
Operating Temperature	Topr	-20 ~ +85	1	℃
Storage Temperature	Tstg	-55 ~ +150	1	℃

Notes

1.If used beyond the absolute maximum ratings, FT5x26 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2.Make sure VDDA(high)≥VSSA (low)
3.Make sure VDD (high)≥VSS (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=VDD3=2.8~3.6V, Ta=-20~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	--	IOVCC	V	
Input low -level voltage	VIL		-0.3	--	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	--	--	V	
Output low -level voltage	VOL	IOH=0.1mA	--	--	0.3 x IOVCC	V	
I/O leakage current	ILI	Vin=0~VDDA	-1	--	1	μA	
Current consumption （Normal operation mode）	Iopr	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	mA	
Current consumption （Monitor mode）	Imon	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	mA	
Current consumption （Sleep mode）	Islp	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	TBD	--	μA	
Step-up output voltage	VDD5	VDDA=VDD3= 2.8V		TBD		V	
Power Supply voltage	VDDA VDD3		2.8		3.6	V	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
OSC clock 1	fosc1	VDD3 = 2.8V Ta=25℃	47	48	49	MHz	

Table 3-4 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		100	150	270	KHz	
TX output rise time	Ttxr		--	20	--	nS	
TX output fall time	Ttxf		--	20	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

3.4 I/O Ports Circuits

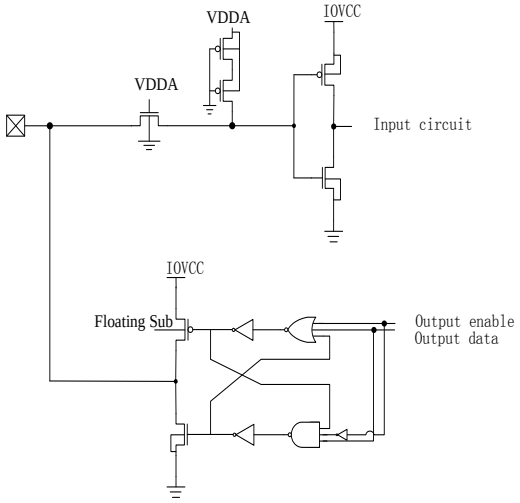


Figure 3-1 Digital In/Out Port Circuit

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

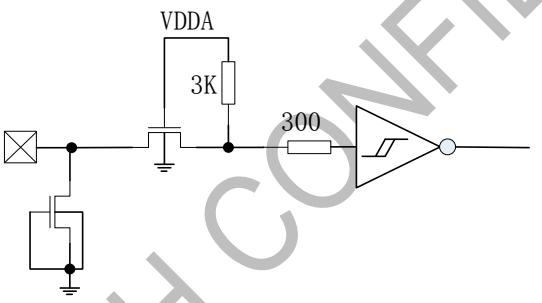


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C/SPI shouldn't be used by other devices during Reset time after IOVCC powering on (Tprt). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

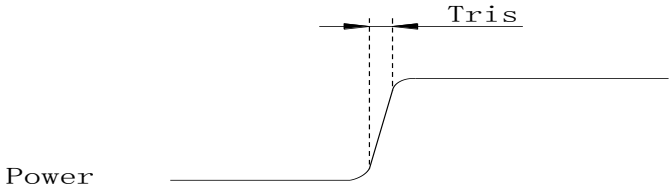


Figure 3-7 Power on time

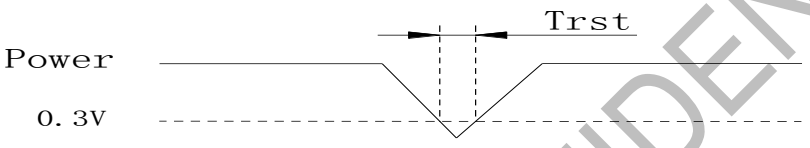


Figure 3-8 Power Cycle requirement

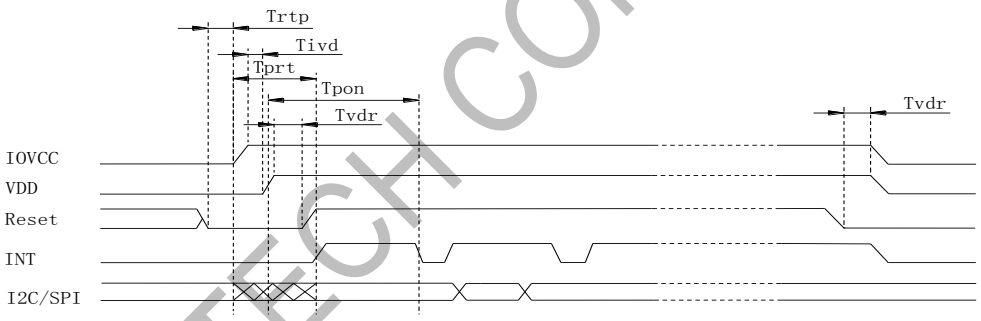


Figure 3-9 Power on / down Sequence

Reset time must be enough to guarantee reliable reset, The time of starting to report point after resetting approach to the time of starting to report point after powering on.

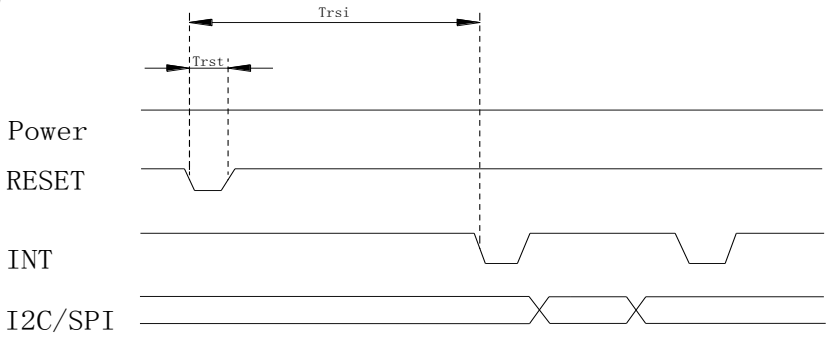


Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC powering on	10	--	μs
Tprt	Reset time after IOVCC powering on	2Tris+Tivd+Tvdr	--	ms
Tpon	Time of starting to report point after powering on	400	--	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	400	--	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

Pin List of FT5x26

Table 4-1 Pin Definition of FT5x26

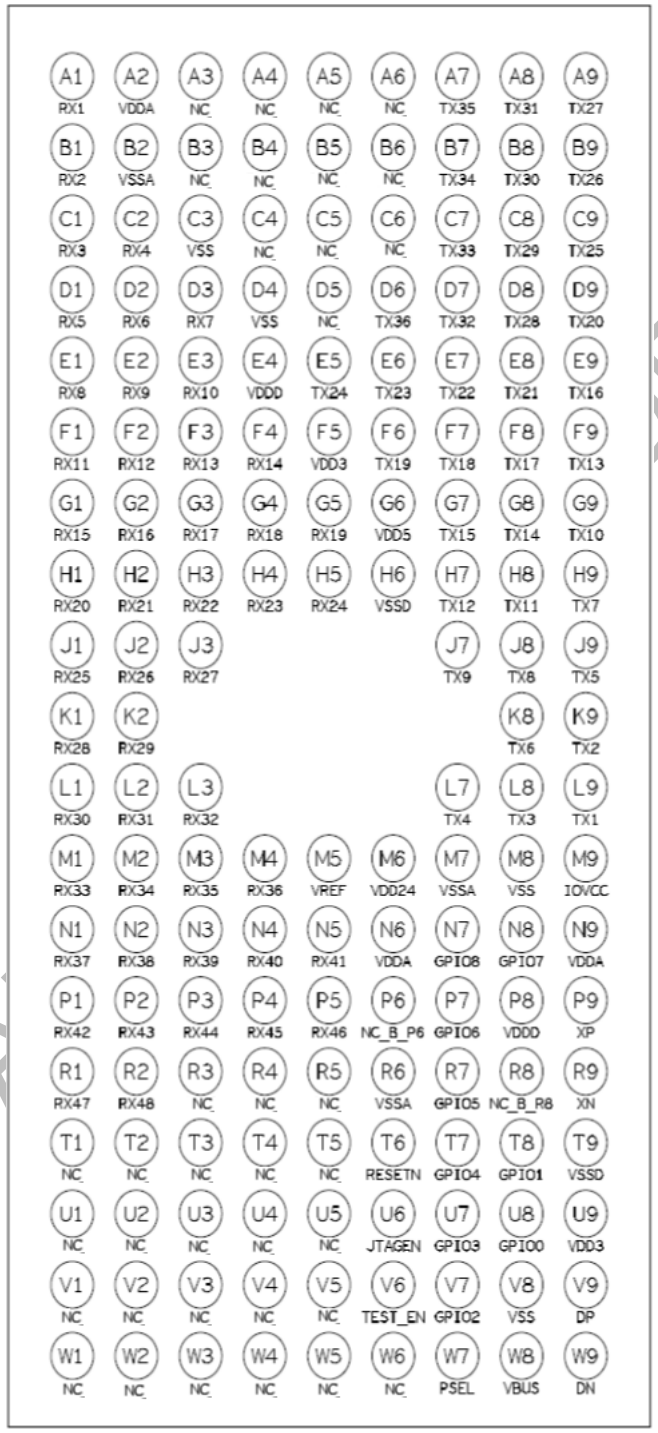
Name	Pin No.				Type	Description
	FT5826QSL	FT5926QSM	FT5B26QSN	FT5C26QSP		
VDDA	A2	A2	A2	A2	PWR	Analog power supply
VSSA	B2	B2	B2	B2	PWR	Analog ground
RX1	A1	A1	A1	A1	I	Receiver input pins
RX2	B1	B1	B1	B1	I	Receiver input pins
RX3	C1	C1	C1	C1	I	Receiver input pins
RX4	C2	C2	C2	C2	I	Receiver input pins
RX5	D1	D1	D1	D1	I	Receiver input pins
RX6	D2	D2	D2	D2	I	Receiver input pins
RX7	D3	D3	D3	D3	I	Receiver input pins
RX8	E1	E1	E1	E1	I	Receiver input pins
RX9	E2	E2	E2	E2	I	Receiver input pins
RX10	E3	E3	E3	E3	I	Receiver input pins
RX11	F1	F1	F1	F1	I	Receiver input pins
RX12	F2	F2	F2	F2	I	Receiver input pins
RX13	F3	F3	F3	F3	I	Receiver input pins
RX14	F4	F4	F4	F4	I	Receiver input pins
RX15	G1	G1	G1	G1	I	Receiver input pins
RX16	G2	G2	G2	G2	I	Receiver input pins
RX17	G3	G3	G3	G3	I	Receiver input pins
RX18	G4	G4	G4	G4	I	Receiver input pins
RX19	G5	G5	G5	G5	I	Receiver input pins
RX20	H1	H1	H1	H1	I	Receiver input pins
RX21	H2	H2	H2	H2	I	Receiver input pins
RX22	H3	H3	H3	H3	I	Receiver input pins
RX23	H4	H4	H4	H4	I	Receiver input pins
RX24	H5	H5	H5	H5	I	Receiver input pins
RX25	J1	J1	J1	J1	I	Receiver input pins

RX26	J2	J2	J2	J2	I	Receiver input pins
RX27	J3	J3	J3	J3	I	Receiver input pins
RX28	K1	K1	K1	K1	I	Receiver input pins
RX29	K2	K2	K2	K2	I	Receiver input pins
RX30	L1	L1	L1	L1	I	Receiver input pins
RX31	L2	L2	L2	L2	I	Receiver input pins
RX32	L3	L3	L3	L3	I	Receiver input pins
RX33	M1	M1	M1	M1	I	Receiver input pins
RX34	M2	M2	M2	M2	I	Receiver input pins
RX35	M3	M3	M3	M3	I	Receiver input pins
RX36	M4	M4	M4	M4	I	Receiver input pins
VDDA	N6	N6	N6	N6	PWR	Analog power supply
VREF	M5	M5	M5	M5	PWR	Generated internal reference voltage. A 1μF ceramic capacitor to ground is required.
VDD24	M6	M6	M6	M6	PWR	Generated internal 2.4V reference voltage. A 1μF ceramic capacitor to ground is required.
VSSA	R6	R6	R6	R6	PWR	Analog ground
RX37	N1	N1	N1	N1	I	Receiver input pins
RX38	N2	N2	N2	N2	I	Receiver input pins
RX39	N3	N3	N3	N3	I	Receiver input pins
RX40	N4	N4	N4	N4	I	Receiver input pins
RX41	N5	N5	N5	N5	I	Receiver input pins
RX42	P1	P1	P1	P1	I	Receiver input pins
RX43	P2	P2	P2	P2	I	Receiver input pins
RX44	P3	P3	P3	P3	I	Receiver input pins
RX45	P4	P4	P4	P4	I	Receiver input pins
RX46	P5	P5	P5	P5	I	Receiver input pins
RX47	R1	R1	R1	R1	I	Receiver input pins
RX48	R2	R2	R2	R2	I	Receiver input pins
RX49		R3	R3	R3	I	Receiver input pins
RX50		R4	R4	R4	I	Receiver input pins
RX51		R5	R5	R5	I	Receiver input pins
RX52		T1	T1	T1	I	Receiver input pins
RX53		T2	T2	T2	I	Receiver input pins
RX54		T3	T3	T3	I	Receiver input pins
RX55		T4	T4	T4	I	Receiver input pins
RX56		T5	T5	T5	I	Receiver input pins
RX57		U1	U1	U1	I	Receiver input pins
RX58		U2	U2	U2	I	Receiver input pins
RX59			U3	U3	I	Receiver input pins
RX60			U4	U4	I	Receiver input pins
RX61			U5	U5	I	Receiver input pins
RX62			V1	V1	I	Receiver input pins
RX63			V2	V2	I	Receiver input pins
RX64			V3	V3	I	Receiver input pins
RX65			V4	V4	I	Receiver input pins

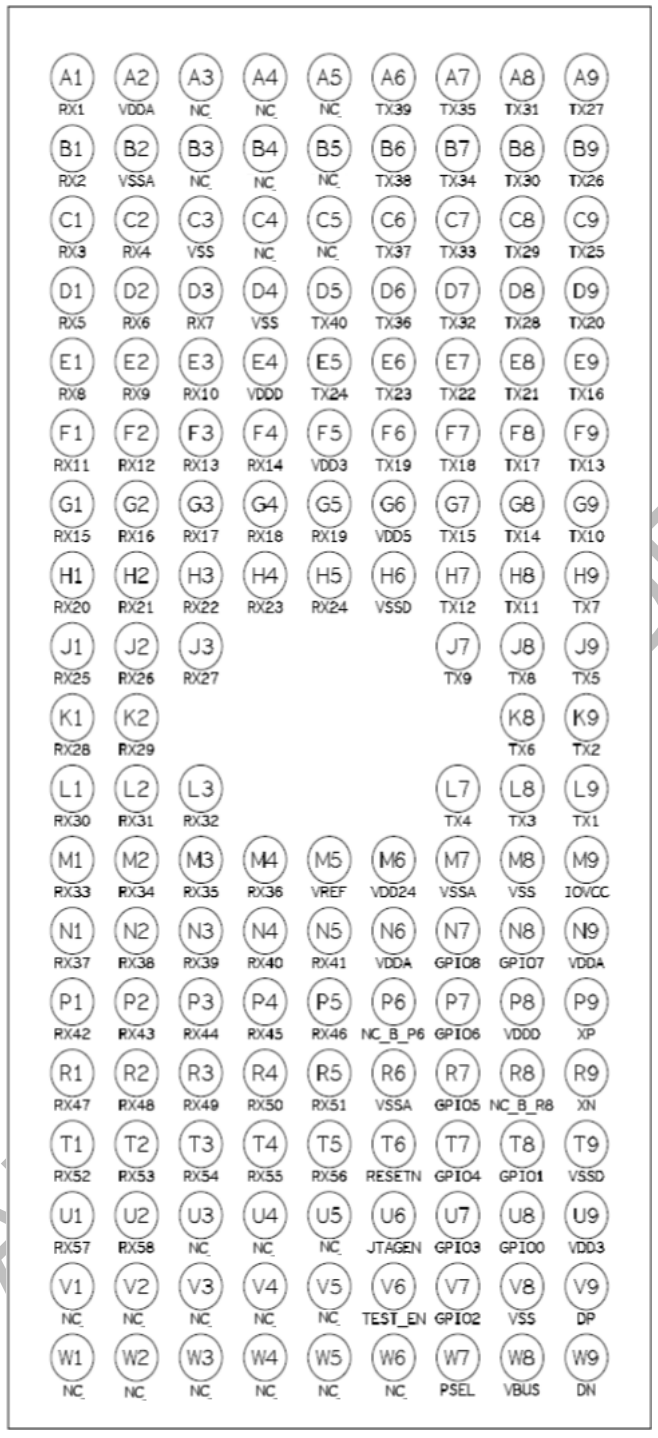
RX66			V5	V5	I	Receiver input pins
RX67				W1	I	Receiver input pins
RX68				W2	I	Receiver input pins
RX69				W3	I	Receiver input pins
RX70				W4	I	Receiver input pins
RX71				W5	I	Receiver input pins
RX72				W6	I	Receiver input pins
VDDA	N9	N9	N9	N9	PWR	Analog power supply
VSSA	M7	M7	M7	M7	PWR	Analog ground
VBUS	W8	W8	W8	W8	PWR	VBUS sensor input, The pin should be connected to USB 4.5~5.5V power supply. This pin must be floating or connected to VDD3 when USB Power is not adopted. A 1 μ F ceramic capacitor to ground is required.
PSEL	W7	W7	W7	W7	I	Power Select pin. PSEL=0, powered by external voltage supply(2.8-3.6V); PSEL=5V(VBUS), powered by USB.
VSS	V8	V8	V8	V8	PWR	Analog ground
DN	W9	W9	W9	W9	I/O	USB D-
DP	V9	V9	V9	V9	I/O	USB D+
XN	R9	R9	R9	R9	I	External Clock Input
XP	P9	P9	P9	P9	O	External Clock Output
VDD3	U9	U9	U9	U9	PWR	Analog power supply
VDDD	P8	P8	P8	P8	PWR	Digital power supply (1.8V), generated internal. A 1 μ F ceramic capacitor to ground is required.
VSSD	T9	T9	T9	T9	PWR	Digital ground
TEST	V6	V6	V6	V6	I	Test pin , should be tie to ground
NC	U6	U6	U6	U6		Not connected
$\overline{\text{RST}}$	T6	T6	T6	T6	I	External Reset, Low is active
TEST_T	N7	N7	N7	N7	I/O	Test PIN
TEST_R	N8	N8	N8	N8	I/O	Test PIN
GPIO6	P7	P7	P7	P7	I/O	General Purpose Input/Output port
GPIO5	R7	R7	R7	R7	I/O	General Purpose Input/Output port
USEL	T7	T7	T7	T7	I/O	Upgrade interface selection low: I2C interface be used high: USB interface be used
MISO	U7	U7	U7	U7	I/O	SPI Slave mode, data output
MOSI	V7	V7	V7	V7	I/O	SPI Slave mode, data input
SDA/SCK	T8	T8	T8	T8	I/O	I2C data input and output/ SPI Slave mode, clock input
SCL/SSEL	U8	U8	U8	U8	I/O	I2C clock input / SPI Slave mode, chip select, active low
IOVCC	M9	M9	M9	M9	PWR	I/O power supply
VSS	M8	M8	M8	M8	PWR	Analog ground
TX1	L9	L9	L9	L9	O	Transmit output pin
TX2	K9	K9	K9	K9	O	Transmit output pin
TX3	L8	L8	L8	L8	O	Transmit output pin
TX4	L7	L7	L7	L7	O	Transmit output pin
TX5	J9	J9	J9	J9	O	Transmit output pin
TX6	K8	K8	K8	K8	O	Transmit output pin
TX7	H9	H9	H9	H9	O	Transmit output pin

TX8	J8	J8	J8	J8	O	Transmit output pin
TX9	J7	J7	J7	J7	O	Transmit output pin
TX10	G9	G9	G9	G9	O	Transmit output pin
TX11	H8	H8	H8	H8	O	Transmit output pin
TX12	H7	H7	H7	H7	O	Transmit output pin
TX13	F9	F9	F9	F9	O	Transmit output pin
TX14	G8	G8	G8	G8	O	Transmit output pin
TX15	G7	G7	G7	G7	O	Transmit output pin
TX16	E9	E9	E9	E9	O	Transmit output pin
TX17	F8	F8	F8	F8	O	Transmit output pin
TX18	F7	F7	F7	F7	O	Transmit output pin
TX19	F6	F6	F6	F6	O	Transmit output pin
TX20	D9	D9	D9	D9	O	Transmit output pin
TX21	E8	E8	E8	E8	O	Transmit output pin
TX22	E7	E7	E7	E7	O	Transmit output pin
TX23	E6	E6	E6	E6	O	Transmit output pin
TX24	E5	E5	E5	E5	O	Transmit output pin
TX25	C9	C9	C9	C9	O	Transmit output pin
TX26	B9	B9	B9	B9	O	Transmit output pin
TX27	A9	A9	A9	A9	O	Transmit output pin
TX28	D8	D8	D8	D8	O	Transmit output pin
TX29	C8	C8	C8	C8	O	Transmit output pin
TX30	B8	B8	B8	B8	O	Transmit output pin
TX31	A8	A8	A8	A8	O	Transmit output pin
TX32	D7	D7	D7	D7	O	Transmit output pin
TX33	C7	C7	C7	C7	O	Transmit output pin
TX34	B7	B7	B7	B7	O	Transmit output pin
TX35	A7	A7	A7	A7	O	Transmit output pin
TX36	D6	D6	D6	D6	O	Transmit output pin
VDD5	G6	G6	G6	G6	PWR	internal generated 5V power supply， A 1 μF ceramic capacitor to ground is required.
VDD3	F5	F5	F5	F5	PWR	Analog power supply
VSS	D4	D4	D4	D4	PWR	Analog ground
VSSD	H6	H6	H6	H6	PWR	Digital ground
VDDD	E4	E4	E4	E4	PWR	Digital power supply (1.8V), generated internal. A 1 μF ceramic capacitor to ground is required.
TX37		C6	C6	C6	O	Transmit output pin
TX38		B6	B6	B6	O	Transmit output pin
TX39		A6	A6	A6	O	Transmit output pin
TX40		D5	D5	D5	O	Transmit output pin
TX41			C5	C5	O	Transmit output pin
TX42			B5	B5	O	Transmit output pin
TX43			A5	A5	O	Transmit output pin
TX44			C4	C4	O	Transmit output pin
TX45				B4	O	Transmit output pin
TX46				A4	O	Transmit output pin
TX47				B3	O	Transmit output pin

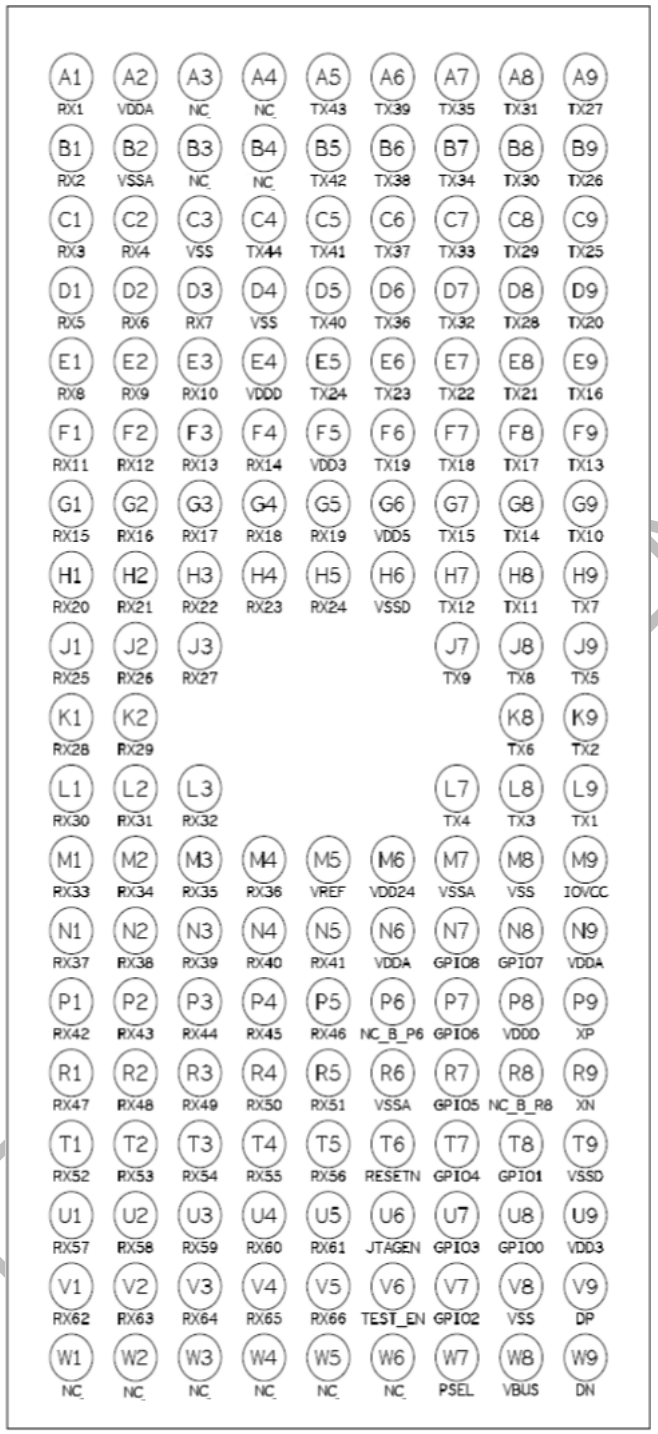
TX48				A3	O	Transmit output pin
VSS	C3	C3	C3	C3	PWR	Analog ground
NC	P6	P6	P6	P6		Not connected
NC	R8	R8	R8	R8		Not connected



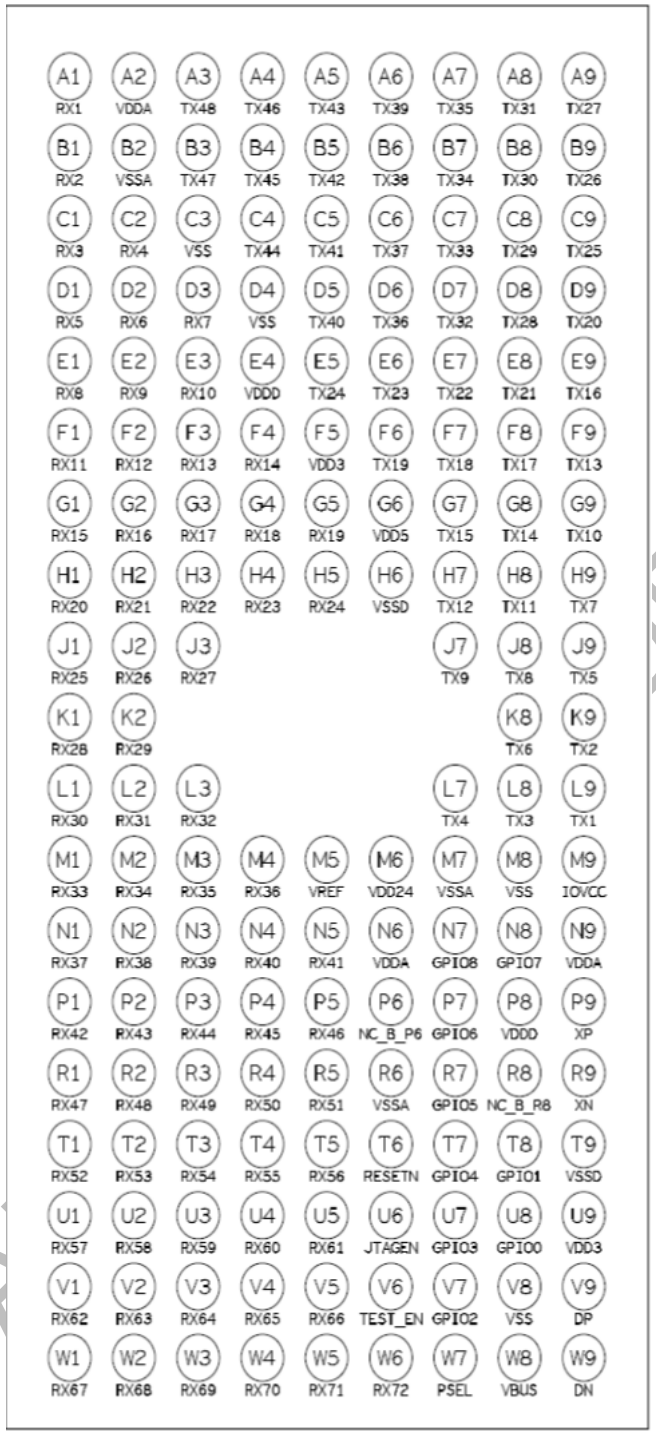
FT5826QSL Package Diagram



FT5926QSM Package Diagram



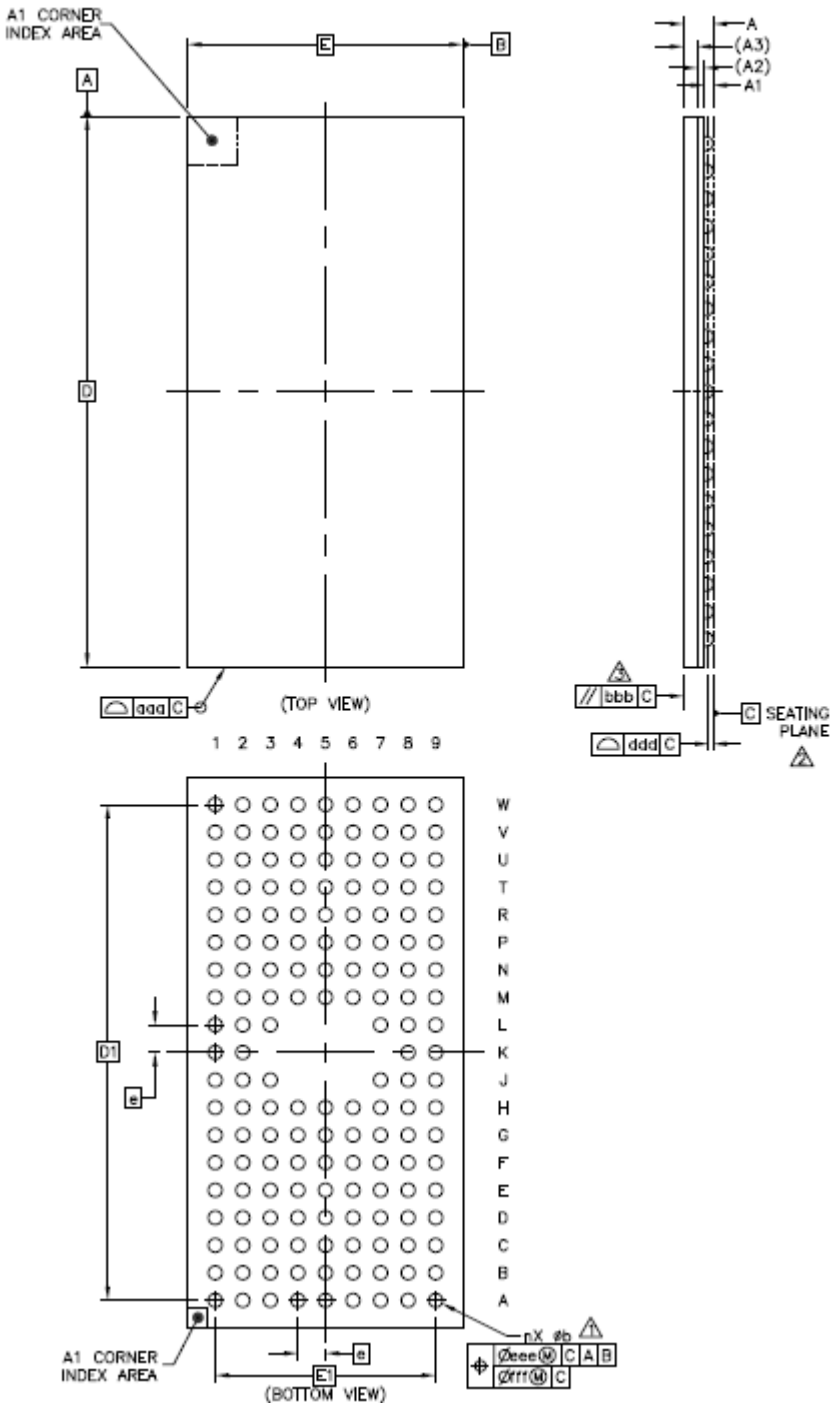
FT5B26QSN Package Diagram



FT5C26QSP Package Diagram

5 PACKAGE INFORMATION

5.1 Package Information of BGA-10x5-160L Package



Item	SYMBOL	Millimeter		
		MIN	TYP	MAX
TOTAL THICKNESS	A	----	----	0.6
STAND OFF	A1	0.12	----	0.2
SUBSTRATE THICKNESS	A2	0.125 REF		
MOLD THICKNESS	A3	0.25 REF		
BODY SIZE	D	10 BSC		
	E	5 BSC		
BALL DIAMETER		0.25		
BALL OPENING		0.25		
BALL WIDTH	b	0.2	----	0.3
BALL PITCH	e	0.5		
BALL COUNT	n	160		
EDGE BALL CENTER TO CENTER	D1	9 BSC		
	E1	4 BSC		
BODY CENTER TO CONTACT BALL	SD	---- BSC		
	SE	---- BSC		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ddd	0.08		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.08		

5.1 Order Information

Package Type	BGA
	160Pin (10 * 5)
	0.6 - P0.5
Product Name	FT5826QSL/FT5926QSM/FT5B26QSN/FT5C26QSP

Note:

1). The last three letters in the product name indicate the package type and lead pitch and thickness.

2). The three last letter indicates the package type.
Q : BGA-10*5

3). The second last letter indicates the lead pitch and thickness.
S : 0.6 - P0.5

4). The last letter indicates the numbers of TX and RX.
L: 36TX-48RX , **M**: 40TX-58RX , **N**: 44TX-66RX, **P**: 48TX-72RX

T: Track Code

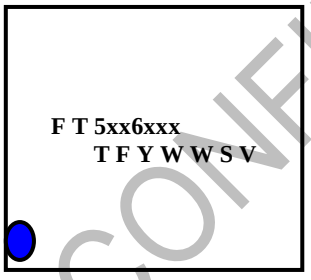
F: "F" for Lead Free process.
"R" for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code

V： IC Version



Product Name	Package Type	# TX Pins	# RX Pins
FT5826QSL	BGA-160L	36	48
FT5926QSM	BGA-160L	40	58
FT5B26QSN	BGA-160L	44	66
FT5C26QSP	BGA-160L	48	72

END OF DATASHEET

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