MSP242X

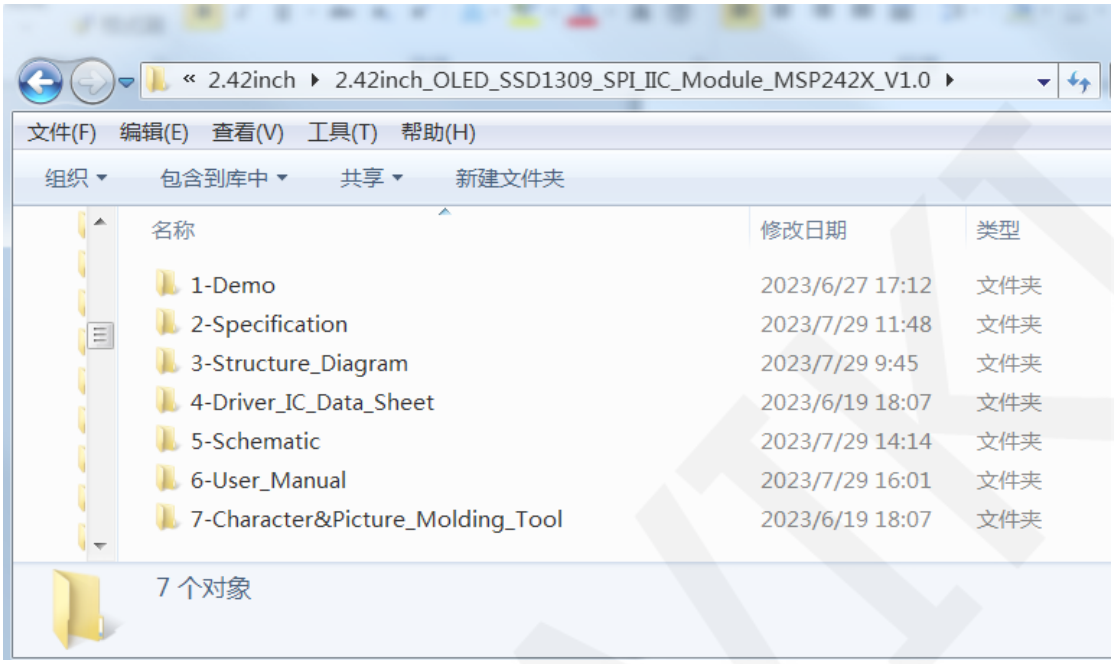
2.42inch OLED SPI&IIC Display Module

User Manual

CONTENTS

1. Rsource Description

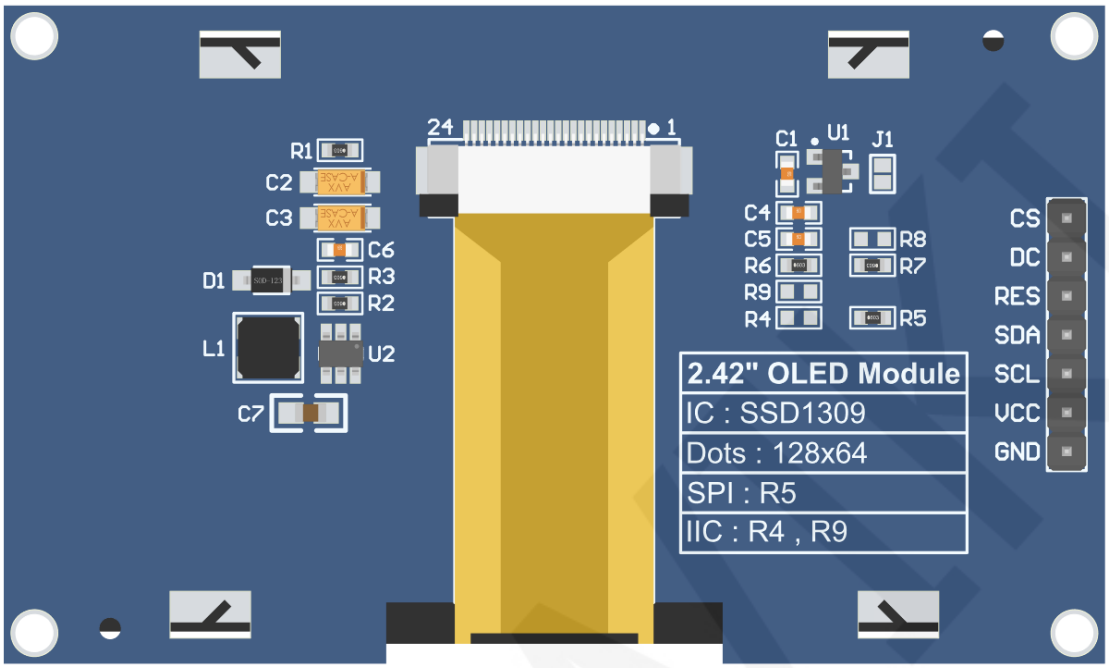
The resource directory is shown in the following figure:



Directory	Content Description
1-Demo	Contains sample programs and usage instructions for each MCU
2-Specification	Including OLED screen specifications and product specifications
3-Structure_Diagram	Includingproduct size structure documents
4-Driver_IC_Data_Sheet	Including OLED screen driver IC Datasheet
5-Schematic	Including product hardware schematic diagram, OLED Altium component diagram, and PCB packaging
6-User_Manual	Contains product user instructions document
7-Character&Picture_Molding_Tool	Contains image extraction software, character extraction software, and software usage instructions. The image and text display tests in the sample program require the use of these two software for mold taking.

2. Interface Description

The interface on the back of the module is shown in the following figure:



NOTE:

A. Connect to a 5V microcontroller, which can short circuit J1 to keep the IO voltage and IO high level consistent;

B. R8 is not soldered by default. If there is no need to control the CS pin, R8 solders the 0R resistor to keep the CS signal grounded;

C. If SPI communication mode is selected, R5 will weld 0R resistor, and R4 and R9 will be disconnected;

D. If IIC communication mode is selected, R4 and R9 will be welded with 0R resistor, and R5 will be disconnected;

Number	Module Pin	Pin Function Description
1	GND	OLED screen power supply ground
2	VCC	OLED screen power supply positive pole (connected to 5V/3.3V)
3	SCL	Using SPI interface: SPI bus clock signal Using IIC interface: IIC bus clock signal
4	SDA	Using SPI interface: SPI bus to write data signals Using IIC interface: IIC bus data signal
5	RES	OLED screen reset control signal, low-level reset (if using

		IIC interface, this pin can be left unchecked and connected to 3.3V high-level)High level: data, low level: command
6	DC	Using SPI interface: OLED screen command/data selection control signal (high level: data, low level: command) Using IIC interface: The IIC bus selects signals from the device address (high level: 0x7A, low level: 0x78, which can be controlled by the master GPIO or connected to 3.3V high level or GND)
7	CS	OLED screen chip selection control signal, effective at low level (if R8 resistor is soldered, this pin can be suspended. If R8 resistor is not soldered, when using IIC interface, this pin must be connected to low level, which can be controlled by master GPIO or GND)

3. Working Principle

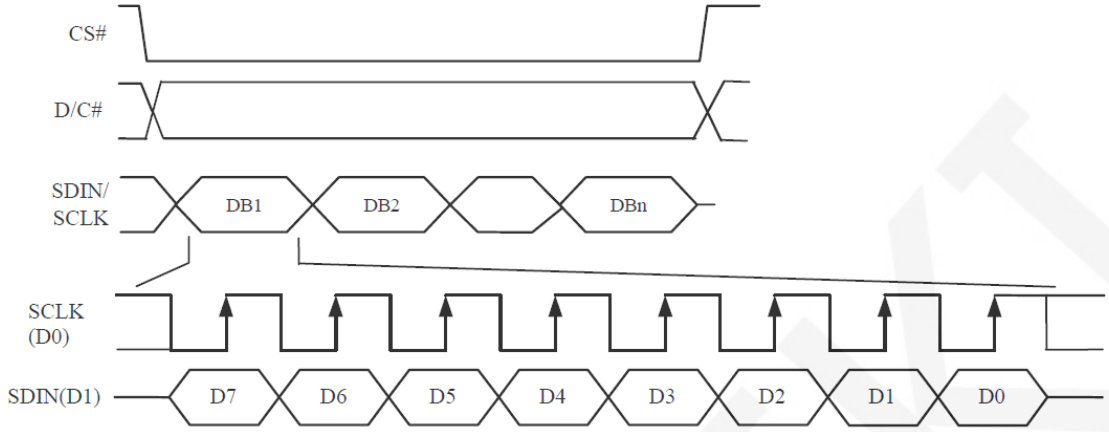
3.1. Introduction to SSD1309 Controller

SSD1309 is an OLED/PLED controller that supports a maximum resolution of 128 * 64 and has a 1024 byte GRAM. Supports 8-bit 6800 and 8-bit 8080 parallel port data buses, as well as 3-wire and 4-wire SPI serial port buses and I2C buses. Due to the large number of IO ports required for parallel control, the most commonly used ones are the SPI serial port bus and I2C bus. It supports vertical scrolling display and can be used for small portable devices such as mobile phones, MP3 players, etc.

The SSD1309 controller uses 1 bit to control the display of one pixel, so each pixel can only display black and white dual colors. The RAM displayed is divided into a total of 8 pages, with 8 rows per page and 128 pixels per row. When setting pixel data, it is necessary to first specify the page address, and then specify the column low address and column high address separately, so 8 vertical pixel points are set simultaneously each time. In order to flexibly control pixel points at any position, the software first sets a global one-dimensional array of the same size as the display RAM. The pixel data is first set to the global array, and this process uses OR, AND operations to ensure that the data previously written to the global array is not damaged. Then, the data of the global array is written to the display RAM, so that it can be displayed through OLED.

3.2. Introduction to SPI Communication Protocol

The writing mode timing of the 4-wire SPI bus is shown in the following figure:



The 4-wire D/C # signal is directly input from the D/C #.

CS # is the slave chip selection signal, and the chip will only be enabled when CS # is at low level.

D/C # is the data/command control signal of the chip. When DC # is used to write commands at low power levels, data is written at high power levels.

SCLK is the SPI bus clock signal, with each rising edge transmitting 1 bit of data;

SDIN writes data signals for the SPI bus, transmitting 8-bit data at a time in a high-order, first transmission manner

For SPI communication, there is a combination of transmission timing, real-time clock phase (CPHA), and clock polarity (CPOL) for data:

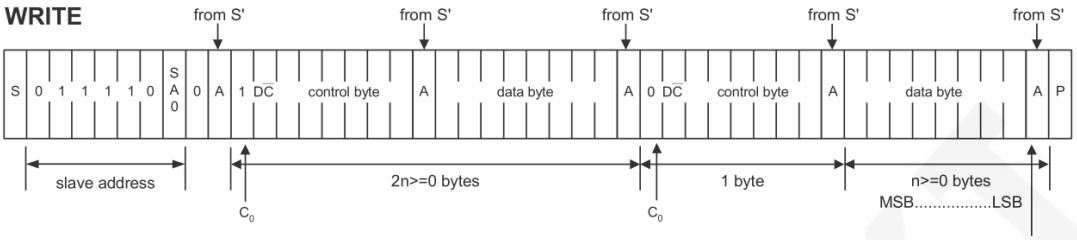
The level of CPOL determines the idle state level of the serial synchronous clock, with CPOL=0, indicating a low level. CPOL pair transmission protocol the discussion did not have much influence;

The height of CPHA determines whether the serial synchronous clock collects data on the first or second clock jump edge,When CPHL=0, perform data collection at the first transition edge;

The combination of these two forms four SPI communication methods, and SPI0 is commonly used in China, where CPHL=0 and CPOL=0.

3.3. Introduction to IIC Communication Protocol

The process of writing data on the IIC bus is shown in the following figure:



After the IIC bus starts working, it first sends the slave device address. After receiving a response from the slave device, it then sends a control byte to notify the slave device. The next data to be sent is a command to write to the IC register or data to write to RAM. After receiving a response from the slave device, it then sends multiple byte values until the transmission is completed and the IIC bus stops working. Among them:

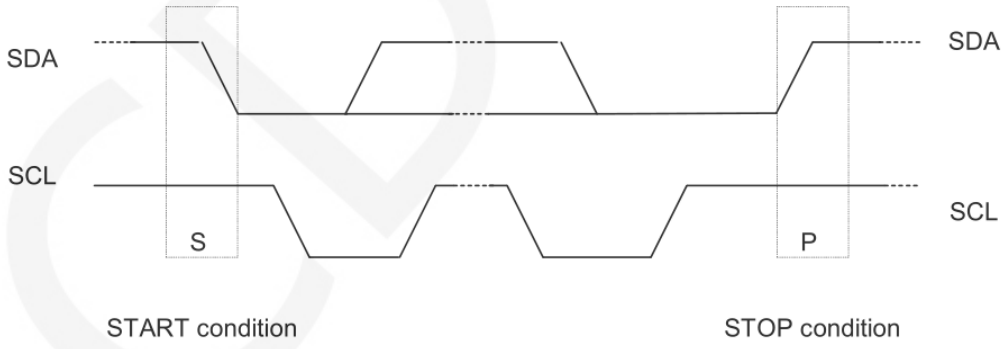
C0=0: This is the last control byte, and the next ones sent are all data bytes

C0=1: The next two bytes to be sent are data bytes and another control byte

D/$\overline{C}$ =0: Register command operation byte

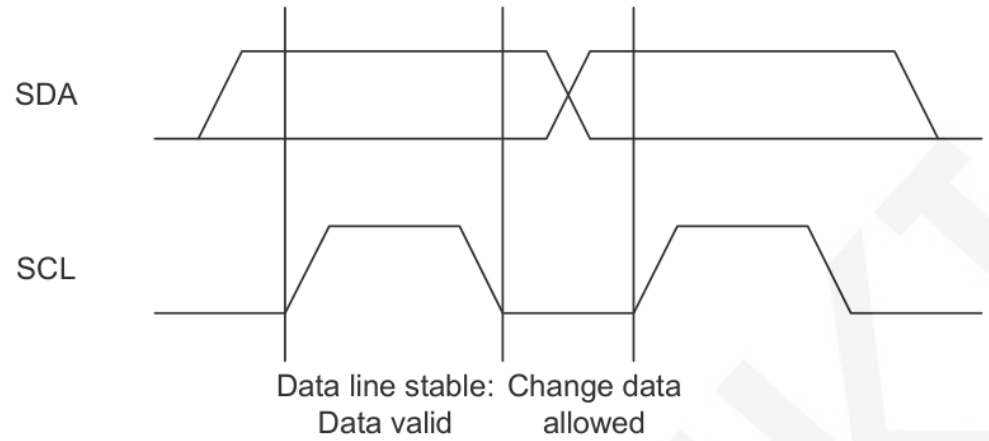
D/$\overline{C}$ =1: Bytes for RAM data operation

The sequence diagram of IIC start and stop is as follows:



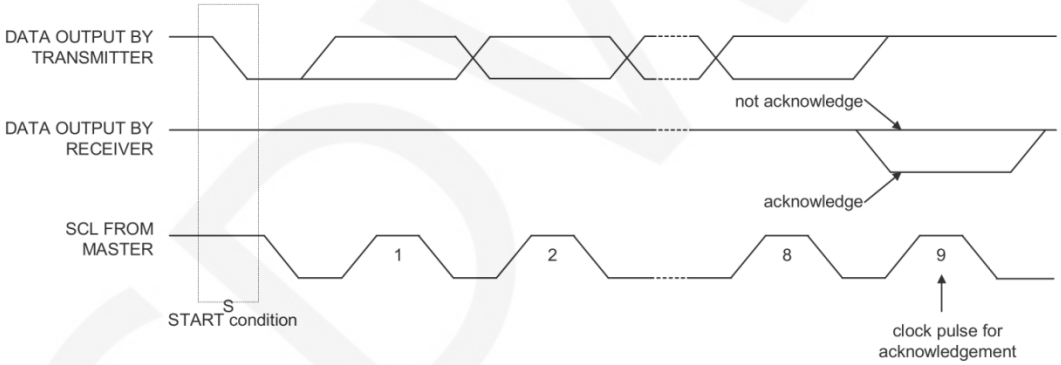
When both the data line and clock line of the IIC remain at high level, the IIC is in an idle state. At this time, the data line changes from high level to low level, and the clock line continues to remain at high level. The IIC bus starts data transmission. At that time, the clock line remained at high level, the data line changed from low level to high level, and the IIC bus stopped data transmission.

The timing chart for IIC to send a bit of data is as follows:



Send 1 bit of data for each clock pulse (the process of pulling up and down). At that time, the clock line was at high power level, and the data line must remain stable. At that time, the clock line was at low power level in order to allow the data line to change.

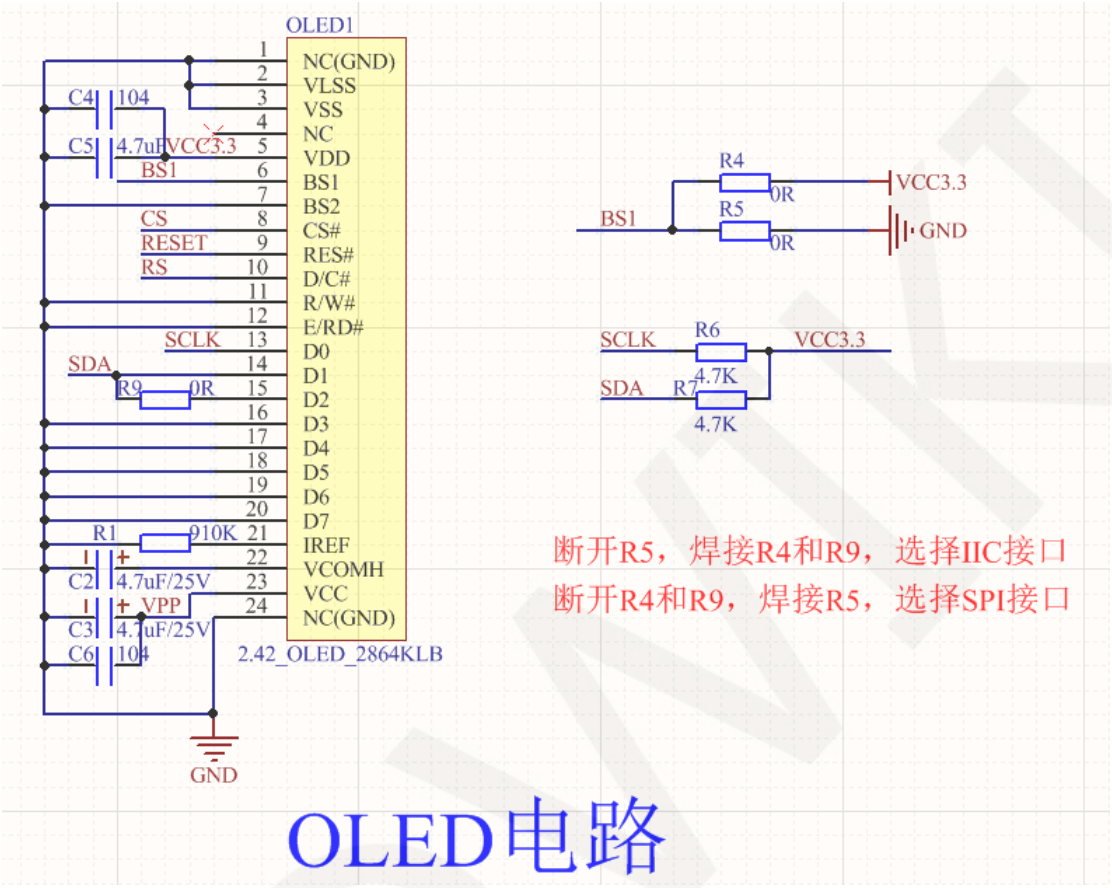
The ACK sending sequence diagram is as follows:



When the master device waits for the ACK from the slave device, it needs to keep the clock line at a high level, and when the slave device sends an ACK, it needs to keep the data line at a low level.

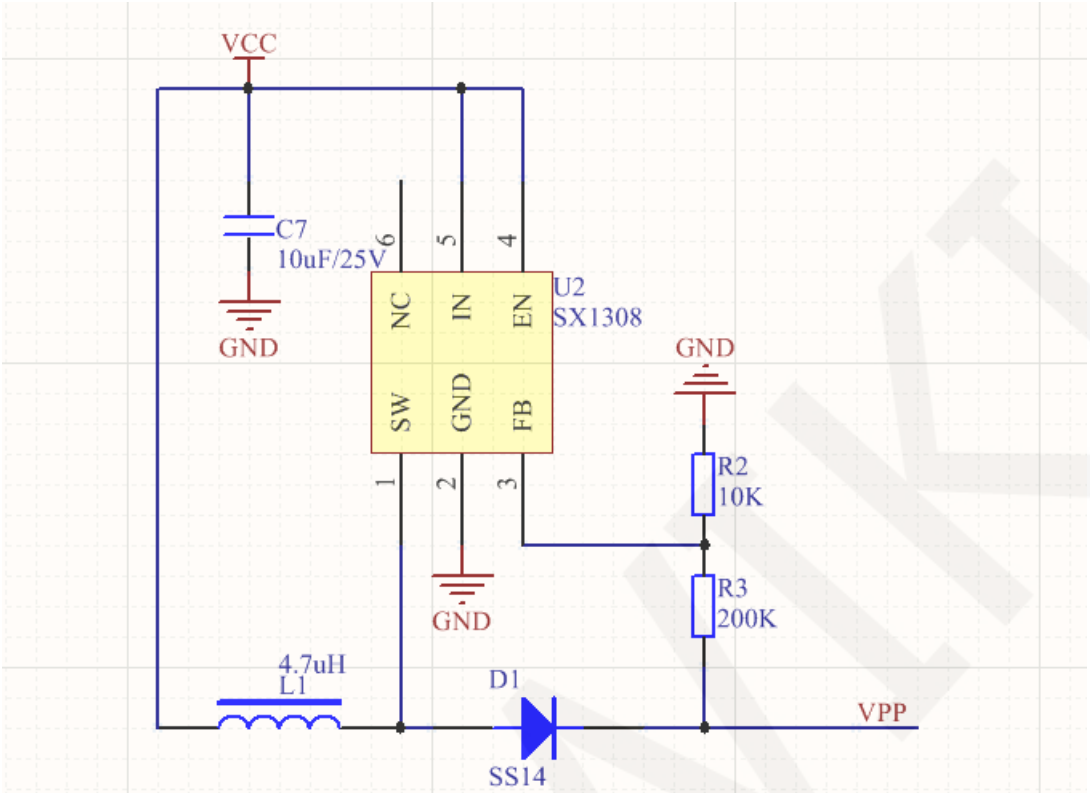
4. Hardware Description

4.1. OLED Display Screen Circuit



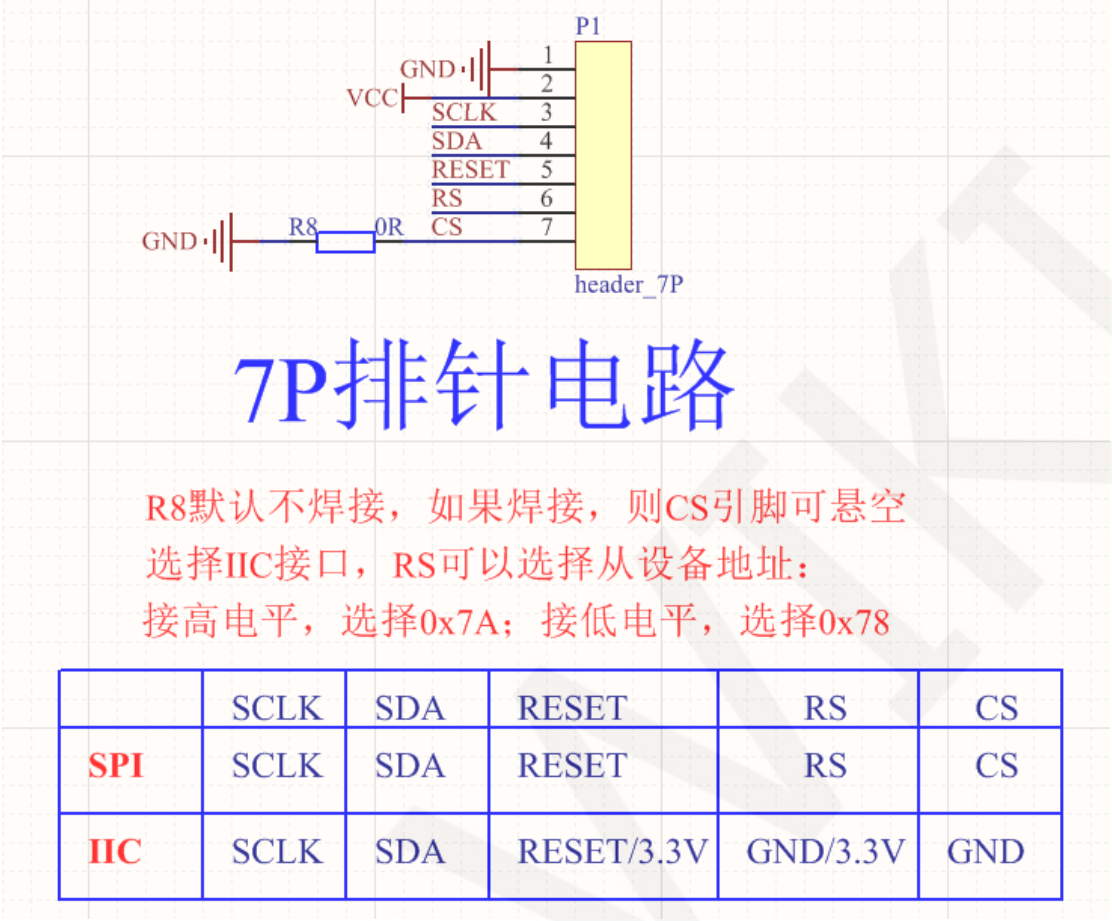
This circuit is an OLED display screen circuit, where OLED1 has a 2.42-inch 24P FPC interface. C2~C6 are bypass capacitors for OLED pins. R6 and R7 are the Pull-up resistor of IIC clock and data pins. R1 is the current limiting resistor of the OLED pixel reference current. R5 represents the switching resistance of the SPI interface, while R4 and R9 represent the switching resistance of the IIC interface. When welding R5 and disconnecting R4 and R9, select the SPI interface; When welding R4 and R9 and disconnecting R5, select the IIC interface. This display module defaults to selecting the SPI interface.

4.2. OLED Extern Power Circuit



This circuit is an OLED external boost circuit, where U2 is an SX1308 boost IC. C7 is the bypass filter capacitor, L1 is the energy storage inductor, and D1 is the diode that prevents reverse direction. R2 and R3 are feedback resistors. SX1308 switches high-frequency through one pin, and L1 and D1 together form an energy storage circuit. 3-pin FB output feedback voltage. By consulting the data manual of SX1308, it can be seen that its feedback voltage is 0.6V. Therefore, the current flowing through R1 and R2 is 0.6/R1, resulting in VPP=(0.6/R1) x (R1+R2), which is calculated to be approximately 12.6V.

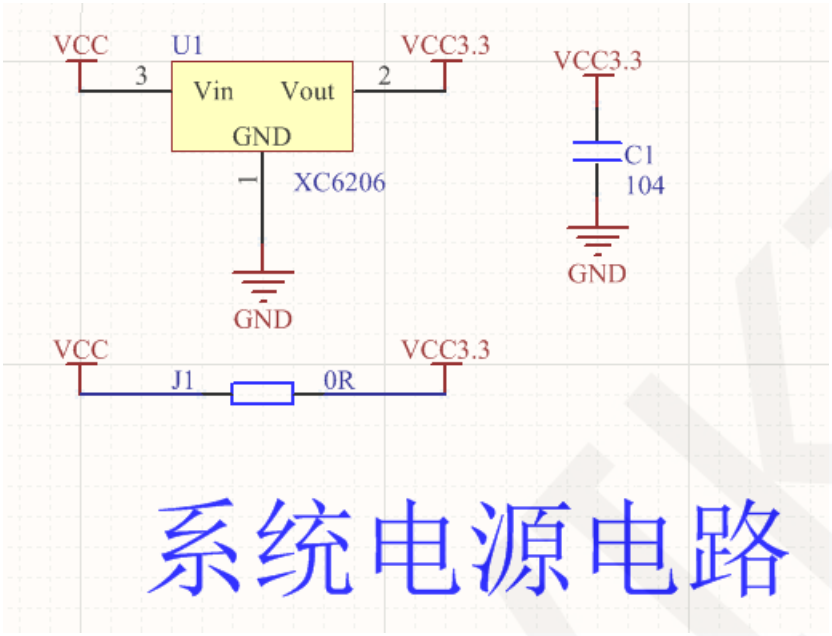
4.3. 7P Pin Interface Circuit



	SCLK	SDA	RESET	RS	CS
SPI	SCLK	SDA	RESET	RS	CS
IIC	SCLK	SDA	RESET/3.3V	GND/3.3V	GND

This is a 7P 2.54mm spacing row pin interface circuit used to connect to the main control. Among them, P1 is the 7P pin, and R8 is the grounding resistance of the CS pin, which is not soldered by default. If R8 is welded, the internal grounding of CS is fixed, and its external pin arrangement can be suspended. When selecting the SPI interface, seven pins, SCLK, SDA, RESET, RS, CS, VCC, and GND, are required. When selecting the IIC interface, the four pins SCLK, SDA, VCC, and GND must be used. Other pins can not be connected to GPIO control, but must be in a fixed state. The RESET pin must be connected to a high level, the RS pin must be determined based on the IIC slave device address, and the CS pin must be connected to a low level. Of course, the GPIO port can also be used to control the status of these pins.

4.4. System Power Circuit



This circuit is a module system power regulator circuit, with U1 as the regulator, which can convert external input 5V or 3.3V voltage into 3.3V output, and C1 as the bypass filter capacitor.

5. Example program usage instructions

For specific instructions, please refer to the example program usage instructions document in the example program directory.

A. Connect the display module to the main control board (directly plug in, use DuPont cable or FPC cable connection);

B. Connect the main control board to the PC (it needs to be connected according to the download method) and power on the main control board;

C. Modify, compile, and download sample programs;

D. Check the display of the module and check if the program runs successfully;

6. Common tool software

The example program needs to display Chinese and English, symbols, and monochrome images, so the mold taking software **PCtoLCD2002** needs to be used.

PCtoLCD2002 is used for text or monochrome image extraction.

The **PCtoLCD2002** mold taking software is set as follows:

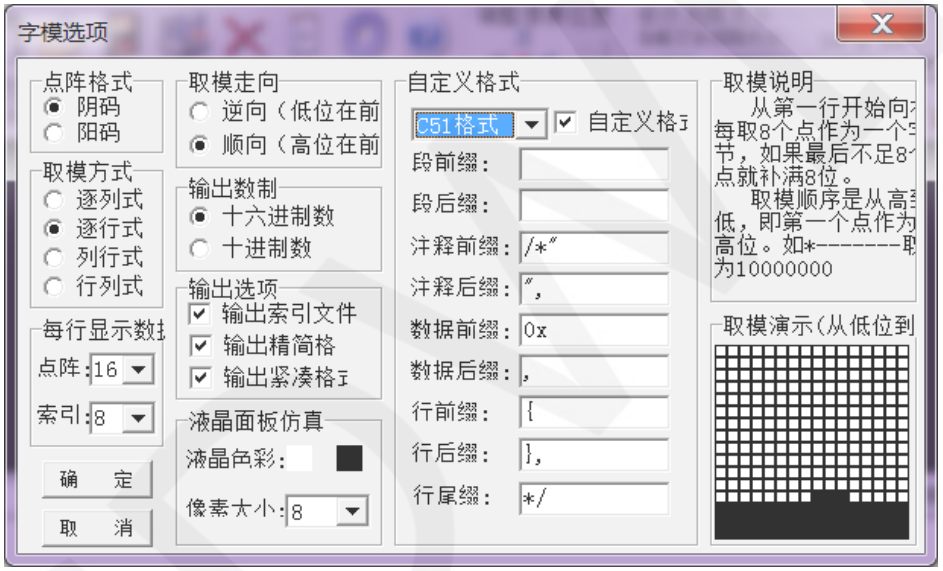
Dot Matrix Format Selection **Yin Code**

Select **row by row mode for mold** taking(C51 test program needs to select Determinant)

Select **the direction of the mold taking direction** in the clockwise direction (with the higher position in front) (C51 testing program needs to select reverse (low order first))

Output Number System Selection **Hexadecimal Number**

Custom Format Selection **C51 Format**



The specific setting method can be found on the following webpage:

http://www.lcdwiki.com/Chinese_and_English_display_modulo_settings