# PRODUCT SPECIFICATIONS

For Customer:_____ ☐ : APPROVAL FOR SPECIFICATION

Customer Model No._____ ☐ : APPROVAL FOR SAMPLE

Module No.: 070BOE102E-L101 Date : 2013.12.06

Version :0

**Table of Contents**



**For Customer's Acceptance:**

| Approved By | Comment |
|---|---|
| | |

| PREPARED | CHECKED | VERIFIED BY QA DEPT | VERIFIED BY R&D DEPT |
|---|---|---|---|
| | | | |

## 2. Revision Record

| Date | Rev.No. | Page | Revision Items | Prepared |
|---|---|---|---|---|
| **2013.12.06** | **V0** | | **The first release** | **Wang** |
| | | | | |

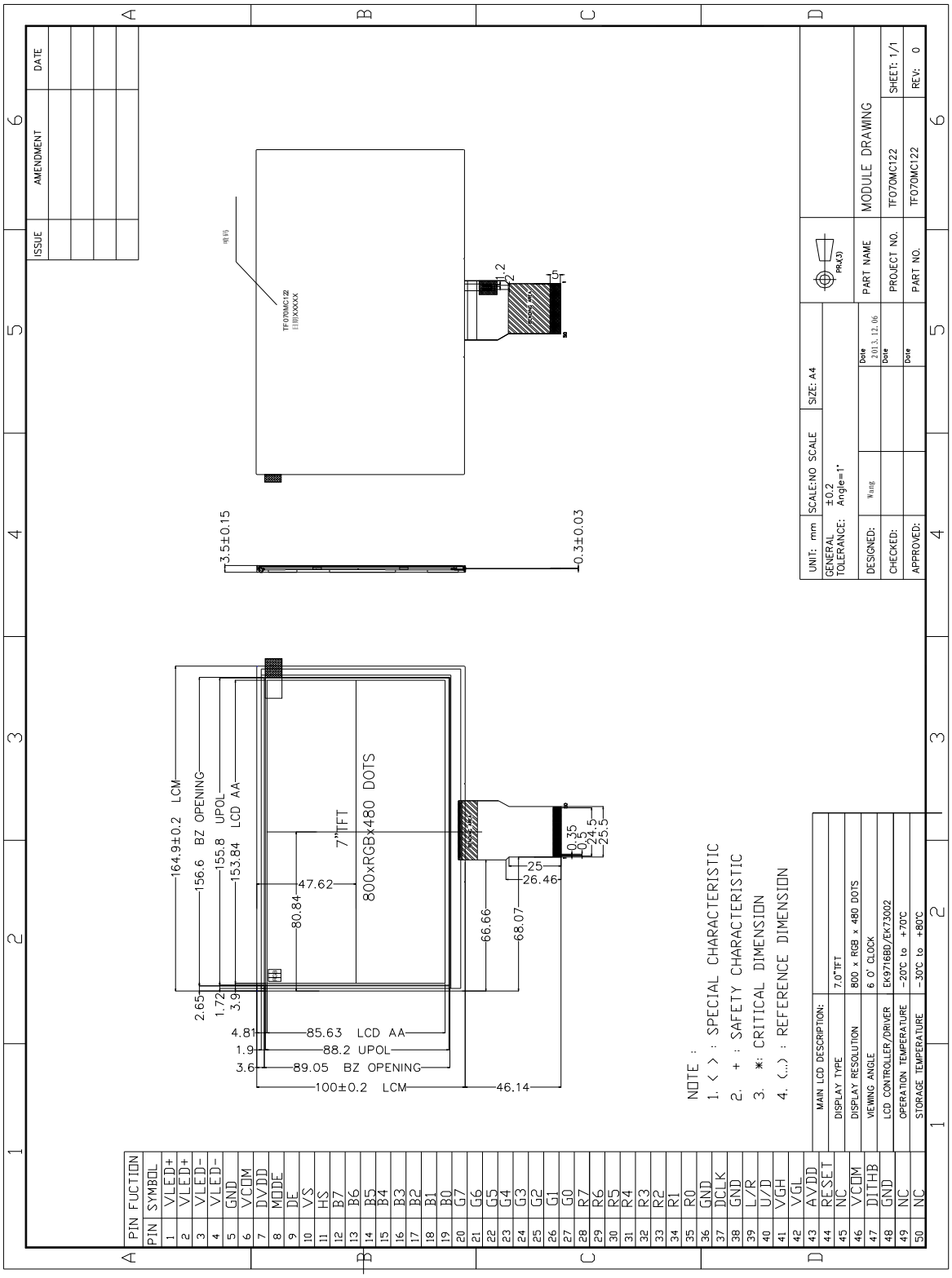
## 3. General Specifications

070BOE102E-L101 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The 7.0″ display area contains 800 x 480 pixels and
can display up to 16M colors. This product accords with RoHS environmental criterion.

| Item | Contents | Unit | Note |
|---|---|---|---|
| LCD Type | TFT | - | |
| Display color | 16M | | 1 |
| Viewing Direction | 6 | O'Clock | |
| Operating temperature | -20~+70 | ℃ | |
| Storage temperature | -30~+80 | ℃ | |
| Module size | Refer to outline drawing | mm | 2 |
| Active Area(W×H) | 153.84 x 85.63 | mm | |
| Number of Dots | 800×RGB×480 | dots | |
| Power Supply Voltage | 1.8 | V | |
| Outline Dimensions | Refer to outline drawing | - | |
| Backlight | 15-LEDs (white) | pcs | |
| Weight | --- | g | |
| Data Transfer | R G B | - | |

Note 1: Color tune is slightly changed by temperature and driving voltage.
Note 2: Without FPC and Solder.

# 4.Outline.Drawing



## 5. Absolute Maximum Ratings(Ta=25℃)

### 5.1 Electrical Absolute Maximum Ratings.(Vss=0V ,Ta=25℃)

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 1.71 | 3.6 | V | 1，2 |
| Logic Signal Input /Output Voltage | $V_{IOVCC}$ | -0.3 | $V_{CC}$+0.5 | V | |
| Power Supply Voltage for LCD | Vop | 0 | 3.6 | V | |
| Current of LED | ILED | 0 | 100 | mA | |

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. $V_{CC}$ >$V_{SS}$ must be maintained.
3. Please be sure users are grounded when handing LCD Module.

### 5.2 Environmental Absolute Maximum Ratings.

| Item | Storage | | Operating | | Note |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| Ambient Temperature | -30℃ | 80℃ | -20℃ | 70℃ | 1,2 |
| Humidity | - | - | - | - | 3 |

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.
   The phenomenon is reversible.
3. Ta<=40℃:85%RH MAX.
   Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

# 6. Electrical Specifications and Instruction Code

## 6.1 Electrical characteristics(Vss=0V ,Ta=25℃)

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Power supply | | VCC | Ta=25℃ | 1.71 | 1.8 | 3.6 | V | |
| Input voltage | 'H' | $V_{IH}$ | $V_{CC}$=2.8V | 0.7$V_{CC}$ | - | $V_{CC}$ | V | |
| | 'L' | $V_{IL}$ | $V_{CC}$=2.8V | 0 | - | 0.3$V_{CC}$ | V | |
| Current Consumption | | $I_{CC1}$ | Normal mode | - | - | - | mA | 2 |
| | | $I_{CC2}$ | Sleep mode | - | 0.03 | 0.09 | mA | 2 |

Note:

1:When an optimum contrast is obtained in transmissive mode.

2: Tested in 1×1 chessboard pattern.

## 6.2 LED backlight specification(VSS=0V ,Ta=25℃)

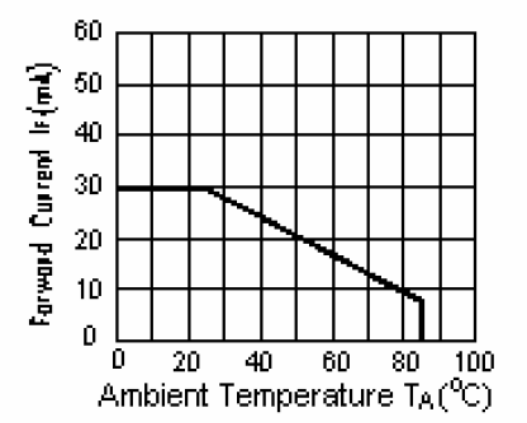
| Item | | Symbol | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Supply voltage | | - | - | - | 9.6 | - | V | 1 |
| Supply current | | $I_f$ | - | - | 100 | - | mA | 2 |
| Forward current | Normal | $I_{pn}$ | 3-chip series x 5 | - | 100 | - | mA | |
| | Dimming | $I_{pd}$ | | - | - | - | | |

Note:

1: $V_{LED}=V_{LED}(+)-V_{LED}(-)$.

2:The current of LED is 20mA.
A LED drive in constant current mode is recommended.

3: LED power consumption is around 0.297W.




CIRCUIT DIAGRAM

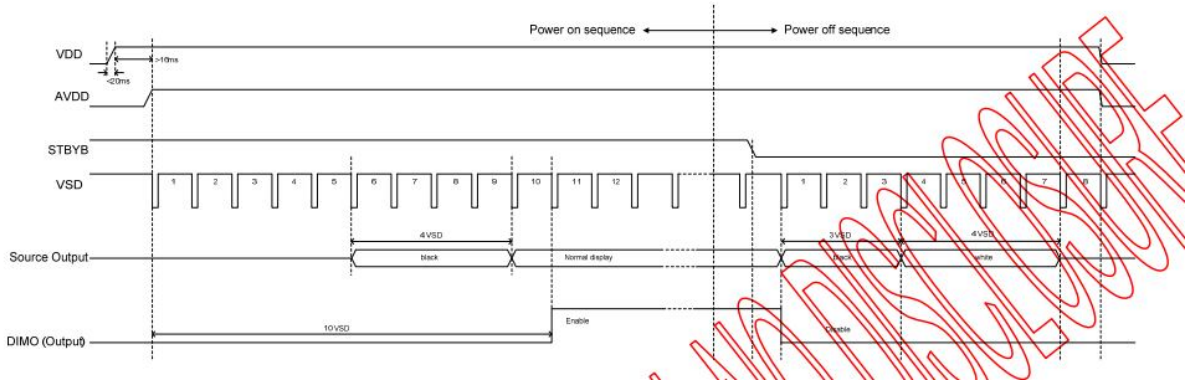
ILED VS TEMP

## 6.3 Interface signals

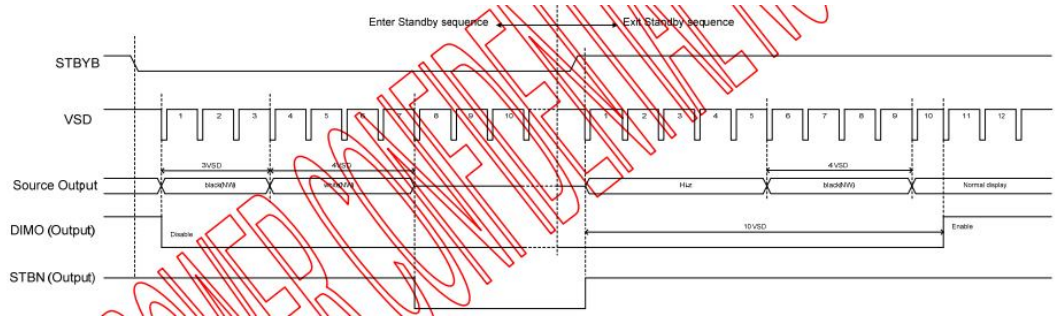
| Pin No. | Symbol | Function |
|---|---|---|
| 1-2 | LED_A | Backlight LED Power |
| 3-4 | LED_K | Backlight LED Ground |
| 5 | GND | Ground |
| 6 | VCOM | Common voltage |
| 7 | DVDD | Power for Digital Circuit |
| 8 | MODE | DE/SYNC mode select |
| 9 | DE | Data Enable Input |
| 10 | VSYNC | Vertical Sync Input |
| 11 | HSYNC | Horizontal Sync Input |
| 12-19 | B7-B0 | Blue Data Bit |
| 20-27 | G7-G0 | Green Data Bit |
| 28-35 | R7-R0 | Red Data Bit / DX0-DX7 |
| 36 | GND | Ground |
| 37 | DCLK | Dot Data Clock |
| 38 | GND | Ground |
| 39 | L/R | Left/Right selection |
| 40 | U/D | Up/Down selection |
| 41 | VGH | Gate ON Voltage |
| 42 | VGL | Gate OFF Voltage |
| 43 | AVDD | Power for Analog Circuit |
| 44 | RESET | Reset pin,This is an active low signal |
| 45 | NC | NC |
| 46 | VCOM | Common voltage |
| 47 | DITHB | Dithering function |
| 48 | GND | Ground |
| 49-50 | NC | NC |

## 6.4 Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time ($T_{POR}$) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

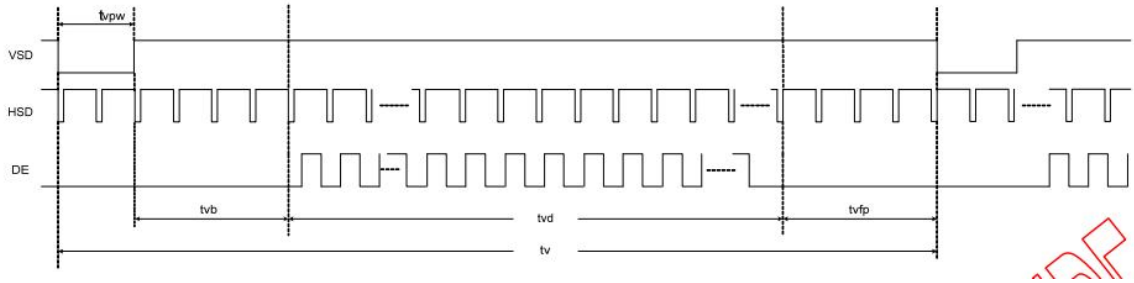



Power-On/Off Timing Sequence

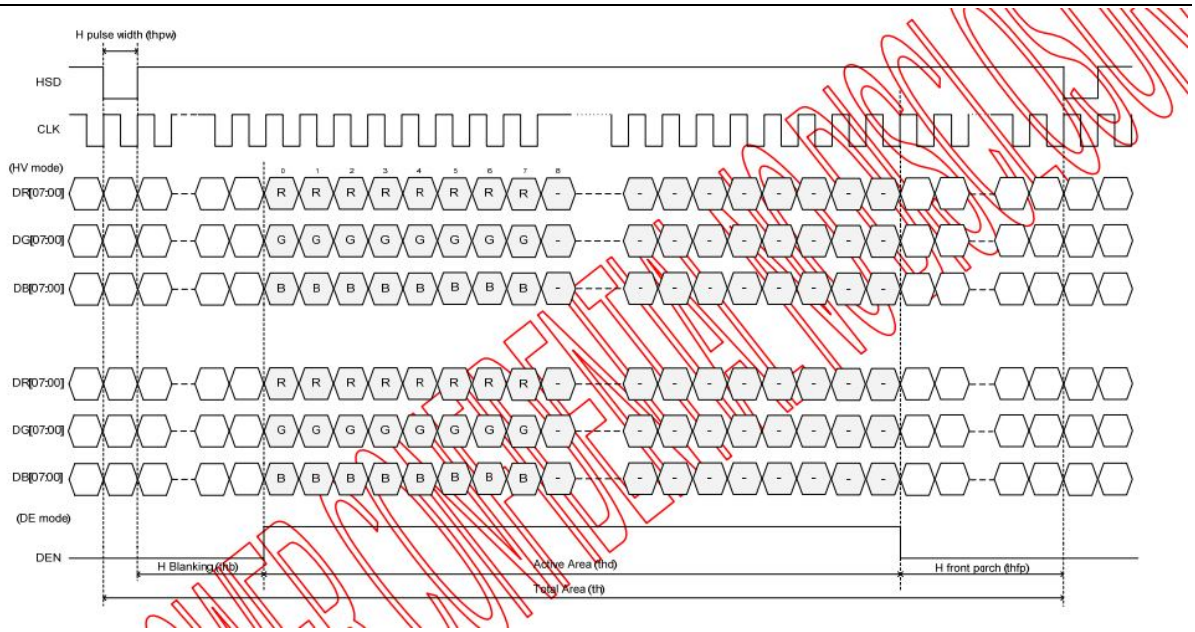



Enter and Exit Standby Mode Sequence

## 6.5 Date Input Format




Vertical input timing




Horizontal input timing

## 6.6 Timing Characteristic

Horizontal input timing

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| Horizontal display area | thd | 800 | | | DCLK | |
| DCLK frequency | fclk | Min. | Typ. | Max | | |
| | | 20 | 33.3 | 50 | MHz | |
| 1 Horizontal Line | th | 908 | 928 | 1088 | DCLK | thb+thpw=88 DCLK is fixed. |
| HSD pulse width | thpw | 1 | 48 | 87 | | |
| HSD Back Porch (Blanking) | thb | 87 | 40 | 1 | | |
| HSD Front Porch | thfp | 20 | 40 | 200 | | |

Vertical input timing

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Vertical display area | tvd | | 480 | | H | |
| VSD period time | tv | 517 | 525 | 712 | H | tvpw+tvb=32H Is fixed |
| VSD pulse width | tvpw | 1 | 1 | 3 | H | |
| VSD Back Porch (Blanking) | tvb | 31 | 31 | 29 | H | |
| VSD Front Porch | tvfp | 5 | 13 | 200 | H | |

## 6.7 DC Characteristics

DC characteristics

(TA = -20 to 85°C, VDD = 1.71 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Low level input voltage | Vil | For the digital circuit | 0 | - | 0.3×VDD | V |
| High level input voltage | Vih | For the digital circuit | 0.7×VDD | - | VDD | V |
| Input leakage current | Ii | For the digital circuit | - | - | ±1 | μA |
| High level output voltage | Voh | Ioh= -400 μA | VDD-0.4 | - | - | V |
| Low level output voltage | Vol | Iol= +400 μA | - | - | VSS+0.4 | V |
| Pull low/high resistor | Ri | For the digital input pin @ VDD=3.3V | 200K | 250K | 300K | ohm |
| Digital Operation current | Idd | Fclk=50 MHz, FLD=48KHz, VDD=3.3V | - | 14 | 18 | mA |
| Digital Stand-by current | Ist1 | Clock and all functions are stopped | - | 10 | 50 | μA |
| Analog Operating Current | Idda | No load, Fclk=50MHz, FLD=48KHz @ VDDA=10V,V1=8V, V14=0.4V | - | 7 | 12 | mA |
| Analog Stand-by current | Ist2 | No load, Clock and all functions are stopped | - | 10 | 50 | μA |
| Input level of V1 ~ V7 | Vref1 | Gamma correction voltage input(Cascade Mode) | 0.4*VDDA | - | VDDA-1 | V |
| Input level of V8 ~ V14 | Vref2 | Gamma correction voltage input(Cascade Mode) | VSSA+1 | - | 0.6*VDDA | V |
| Input level of V1 ~ V7 | Vref3 | Gamma correction voltage input(Dual Gate Mode) | 0.4*VDDA | - | VDDA-0.1 | V |
| Input level of V8 ~ V14 | Vref4 | Gamma correction voltage input(Dual Gate Mode) | VSSA+0.1 | - | 0.6*VDDA | V |
| Output Voltage deviation | Vod1 | Vo = VSSA+0.1V ~ VSSA+0.5V and Vo = VDDA-0.5V ~ VDDA-0.1V | - | ±20 | ±35 | mV |
| Output Voltage deviation | Vod2 | Vo = VSSA+0.5V ~ VDDA-0.5V | - | ±15 | ±20 | mV |
| Output Voltage Offset between Chips | Voc | Vo = VSSA+0.5V ~ VDDA-0.5V | - | - | ±20 | mV |
| Dynamic Range of Output | Vdr | SO1 ~ SO1200 | 0.1 | - | VDDA-0.1 | V |
| Sinking Current of Outputs | IOLy | SO1 ~ SO1200; Vo=0.1V v.s 1.0V , VDDA=13.5V | 80 | - | - | uA |
| Driving Current of Outputs | IOHy | SO1 ~ SO1200; Vo=13.4V v.s 12.5V , VDDA=13.5V | 80 | - | - | uA |
| Resistance of Gamma Table | Rg | Rn: Internal gamma resistor | 0.7*Rn | 1.0*Rn | 1.3*Rn | ohm |

## 6.8 AC Characteristics

AC characteristics

(TA = -20 to 85°C, VDD = 1.71 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

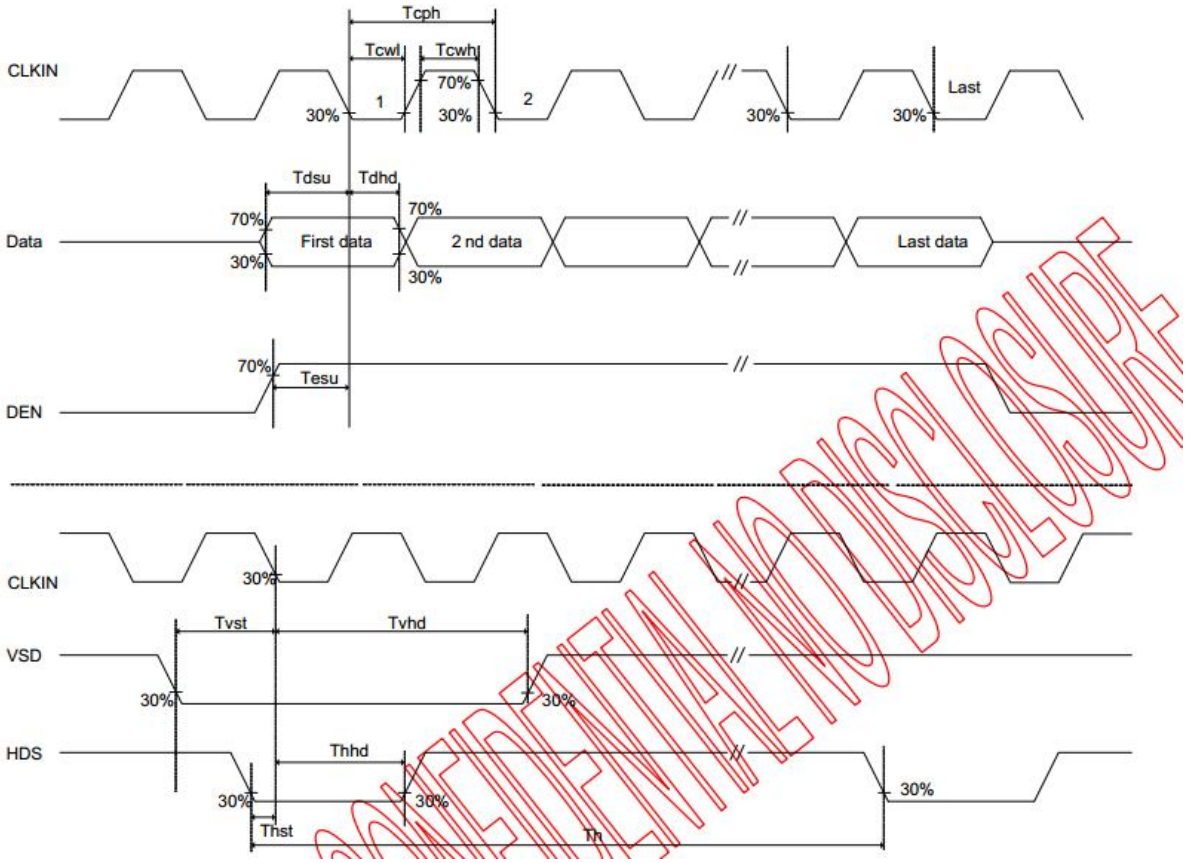
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD Power On Slew rate | $T_{POR}$ | From 0V to 90% VDD | - | - | 20 | ms |
| RSTB pulse width | $T_{RST}$ | CLKIN = 50MHz | 50 | - | - | us |
| CLKIN cycle time | Tcph | - | 20 | - | - | ns |
| CLKIN pulse duty | Tcwh | - | 40 | 50 | 60 | % |
| VSD setup time | Tvst | - | 8 | - | - | ns |
| VSD hold time | Tvhd | - | 8 | - | - | ns |
| HSD setup time | Thst | - | 8 | - | - | ns |
| HSD hold time | Thhd | - | 8 | - | - | ns |
| Data set-up time | Tdsu | DR[7:0], DG[7:0], DB[7:0] to CLKIN | 8 | - | - | ns |
| Data hold time | Tdhd | DR[7:0], DG[7:0], DB[7:0] to CLKIN | 8 | - | - | ns |
| DEN setup time | Tesu | - | 8 | - | - | ns |
| DEN hold time | Tehd | - | 8 | - | - | ns |
| Output stable time | Tsst | 10% to 90% target voltage. CL=120pF, R=10K ohm | - | - | 6 | us |

## 6.8 Timing Table

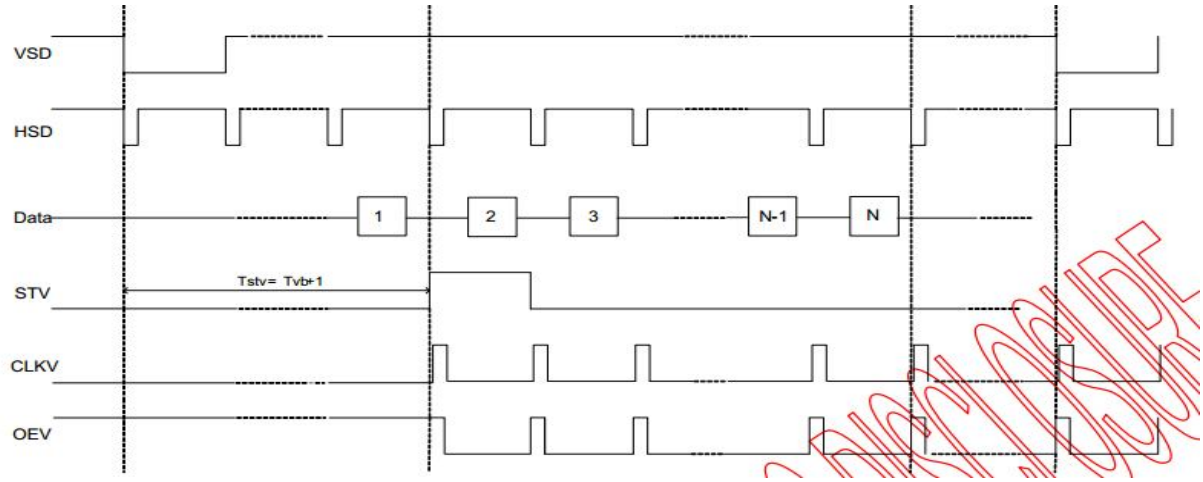
Parallel 24-bit RGB Mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CLKIN Frequency | Fclk | VDD = 1.71V ~3.6V | - | 40 | 50 | MHz |
| CLKIN Cycle Time | Tclk | - | 20 | 25 | - | ns |
| CLKIN Pulse Duty | Tcwh | Tclk | 40 | 50 | 60 | % |
| Time from HSD to Source Output | Thso | | - | 46 | - | CLKIN |
| Time from HSD to LD | Thld | | - | 46 | - | CLKIN |
| Time from HSD to STV | Thstv | | - | 2 | - | CLKIN |
| Time from HSD to CKV | Thckv | - | - | 20 | - | CLKIN |
| Time from HSD to OEV | Thoev | - | - | 4 | - | CLKIN |
| LD Pulse Width | Twld | | | 10 | | CLKIN |
| CKV Pulse Width | Twckv | - | - | 66 | - | CLKIN |
| OEV Pulse Width | Twoev | - | - | 74 | - | CLKIN |

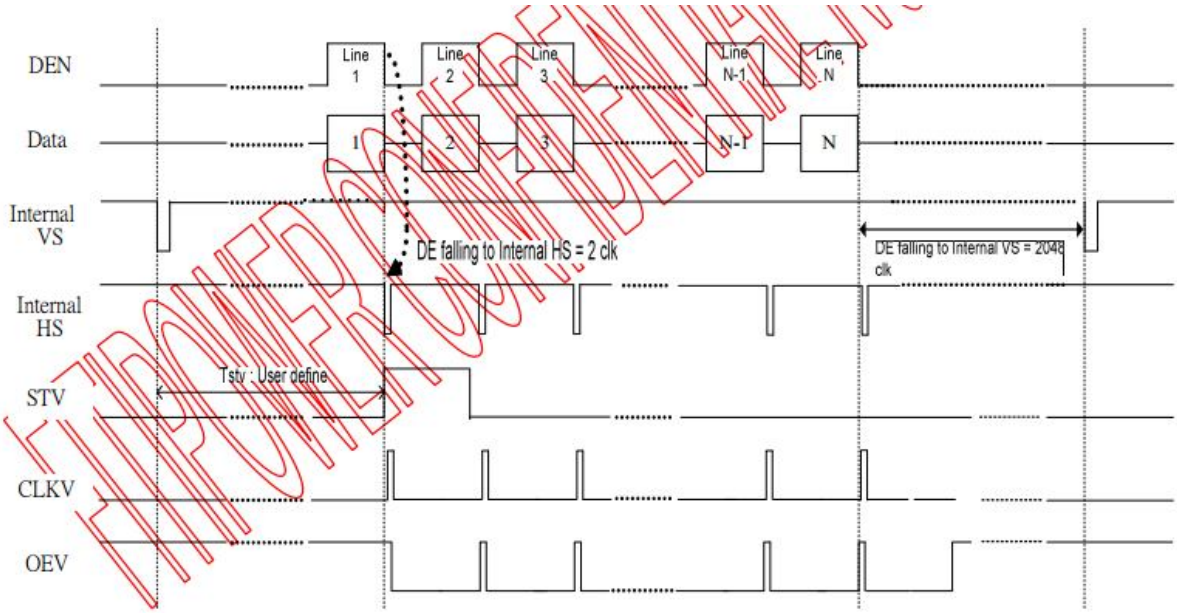
## 6.9 Timing Waveform




Input Clock and Data Timing Diagram




Vertical Timing Diagram HV




Vertical Timing Diagram DE

## 7. Optical Characteristics

| Item | Symbol | **Condition** | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Brightness | Bp | | $\theta$=0° Φ=0° | - | 180 | - | Cd/m$^2$ | 1 |
| Uniformity | ⊿Bp | | | 75 | 80 | - | % | 1,2 |
| Viewing Angle | 3:00 | | Cr≥10 | 60 | 70 | - | Deg | 3 |
| | 6:00 | | | 60 | 70 | - | | |
| | 9:00 | | | 60 | 70 | - | | |
| | 12:00 | | | 50 | 60 | - | | |
| Contrast Ratio | Cr | | $\theta$=0° Φ=0° | 350 | 500 | | - | 4 |
| Response Time | $T_r$+$T_f$ | | | | 25 | | ms | 5 |
| Color of CIE Coordinate | W | x | $\theta$=0° Φ=0° | 0.269 | 0.299 | 0.329 | - | 1,6 |
| | | y | | 0.308 | 0.338 | 0.368 | - | |
| | | Y | | - | - | - | | |
| | R | x | | 0.562 | 0.592 | 0.622 | - | |
| | | y | | 0.289 | 0.319 | 0.349 | - | |
| | | Y | | - | - | - | | |
| | G | x | | 0.279 | 0.309 | 0.339 | - | |
| | | y | | 0.537 | 0.567 | 0.597 | - | |
| | | Y | | - | - | - | | |
| | B | x | | 0.117 | 0.147 | 0.177 | - | |
| | | y | | 0.120 | 0.150 | 0.180 | - | |
| | | Y | | - | - | - | | |
| NTSC Ratio | S | | | - | 50 | - | % | |

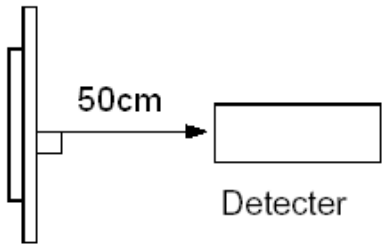
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

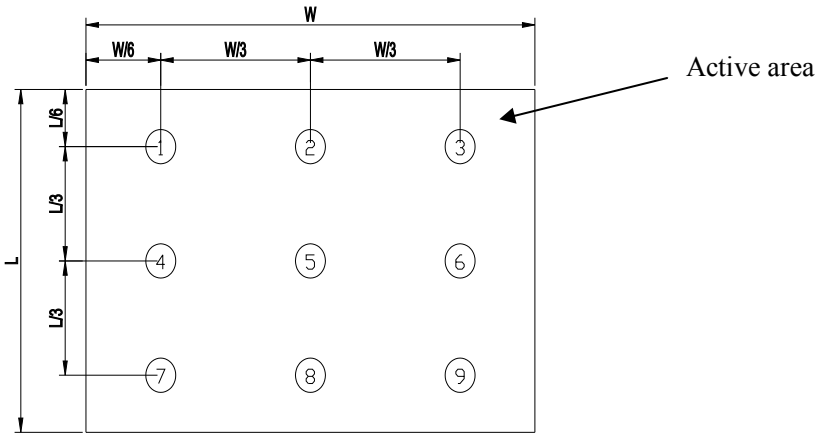



Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

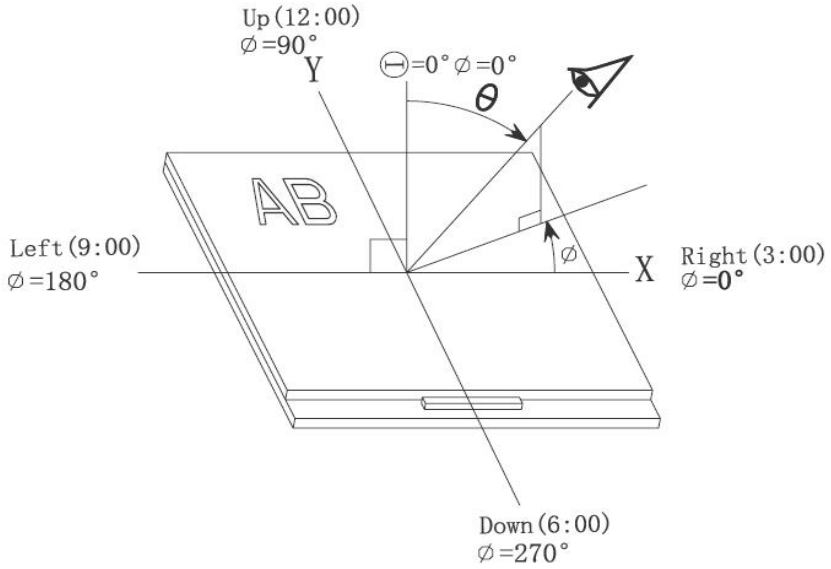
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

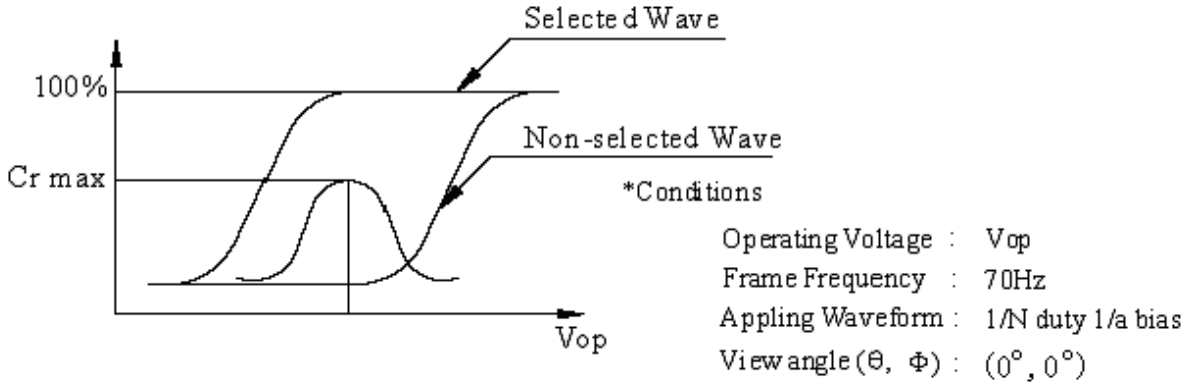



Note 3: The definition of viewing angle:

Refer to the graph below marked by $\theta$ and $\Phi$



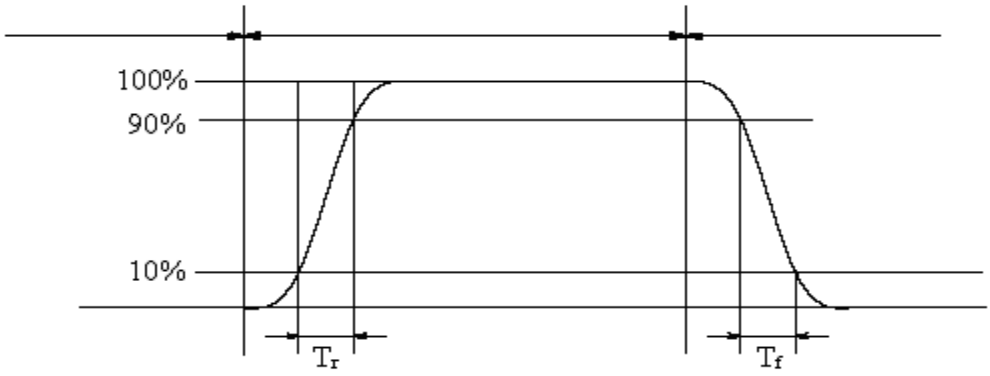

Note 4: Definition of contrast ratio.( Test LCD using DMS501)




$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

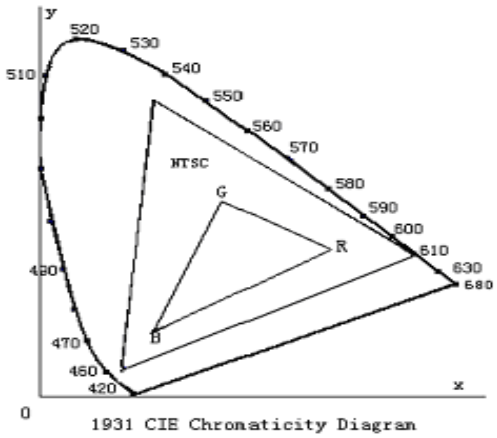
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.




The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

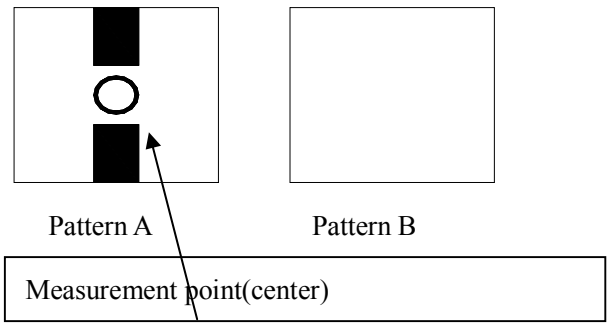



**Color gamut:**

$$S = \frac{\textbf{area of RGB triangle}}{\textbf{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.

Cross talk ratio(%)= | pattern A Brightness-pattern B Brightness | /pattern A Brightness*100




Electric volume value=3F+/-3Hex

## 8. Reliability Test Items and Criteria

| No | Test Item | Test condition | Criterion |
|---|---|---|---|

| | | | |
|---|---|---|---|
| 1 | High Temperature Storage | 80℃±2℃ 96H<br>Restore 2H at 25℃<br>Power off | 1. After testing, cosmetic and electrical defects should not happen.<br>2. Total current consumption should not be more than twice of initial value. |
| 2 | Low Temperature Storage | -30℃±2℃ 96H<br>Restore 2H at 25℃<br>Power off | |
| 3 | High Temperature Operation | 70℃±2℃ 96H<br>Restore 2H at 25℃<br>Power on | |
| 4 | Low Temperature Operation | -20℃±2℃ 96H<br>Restore 4H at 25℃<br>Power on | |
| 5 | High Temperature/Humidity Operation | 60℃±2℃ 90%RH 96H<br>Power on | |
| 6 | Temperature Cycle | –30℃←——→80℃<br>30min 5min 30min<br>after 5 cycle, Restore 2H at 25℃<br>Power off | |
| 7 | Vibration Test | 10Hz~150Hz, 100m/s$^2$, 120min | Not allowed cosmetic and electrical defects. |
| 8 | Shock Test | Half- sine wave,300m/s$^2$,11ms | |
| 9 | ESD Test | Air discharge:+/-8KV,<br>Contact discharge:4KV | |

Note: Operation: Supply 2.8V for logic system.

The inspection terms after reliability test, as below

| ITEM | Inspection |
|---|---|
| Contrast | CR>50% |
| IDD | IDD<200% |
| Brightness | Brightness>60% |
| Color Tone | Color Tone+/-0,05 |

# 9 Quality level

## 9.1 Classification of defects

Major defects (MA): A major defect refers to a defect that may substantially degrade usability for product applications, including all functional defects(such as no display, abnormal display, open or missing segment, short circuit, missing component), outline dimension beyond the drawing, progressive defects and those affecting reliability.

Minor defects (MI): A minor defect refers to a defect which is not considered to be

able to substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation, such as black spot, white spot, bright spot, pinhole, black line, white line, contrast variation, glass defect, polarizer defect, etc.

### 9.2 Definition of inspection range

For dot defect of TFT LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area : center of viewing area

B area : periphery of viewing area

C area : Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area

B zone : Outside Viewing area

X1(A.A~V.A): 2mm X2(A.A~V.A): 2mm

Y1(A.A~V.A): 2mm Y2(A.A~V.A): 2mm

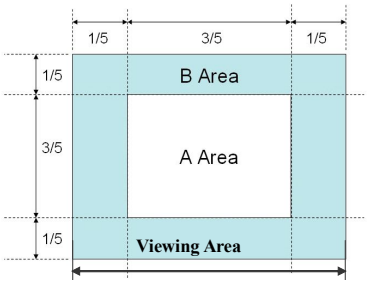



Figure 1

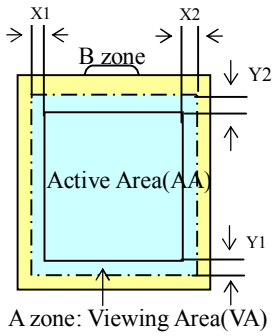



Figure 2

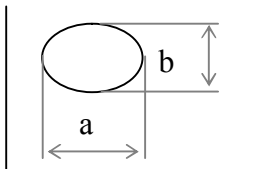
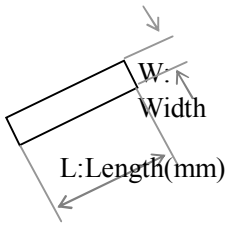
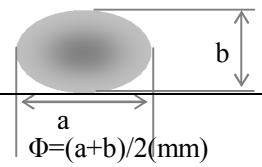
### 9.3 Inspection items and general notes

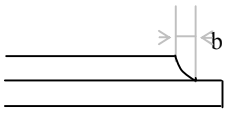
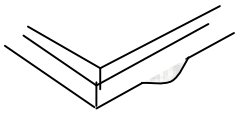
| | | |
|---|---|---|
| General notes | 1.Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and TIANMA.<br>2.Viewing area should be the area which TIANMA guarantees.<br>3.Limit sample should be prior to this Inspection standard.<br>4.Viewing judgment should be under static pattern.<br>5.Inspection conditions<br>Inspection distance: 250 mm (from the sample) Temperature : 25±5 ºC<br>Inspection angle : 45 degrees in 6 o′clock direction (all defects in viewing area should be inspected from this direction) | |
| Inspection items | Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble | The color of a small area is different from the remainder. The phenomenon doesn't change with voltage |
| | Contrast variation | The color of a small area is different from the remainder. The phenomenon changes with voltage |
| | Polarizer defect | Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass |
| | Dot defect (TFT LCD) | The pixel appears bright or dark abnormally when display |
| | Functional defect | No display, Abnormal display, Open or missing segment, Short circuit, False viewing direction |
| | Glass defect | Glass crack, Shaved corner of glass, Surplus glass |
| | PCB defect | Components assembly defect |

## 9.4 Outgoing Inspection level

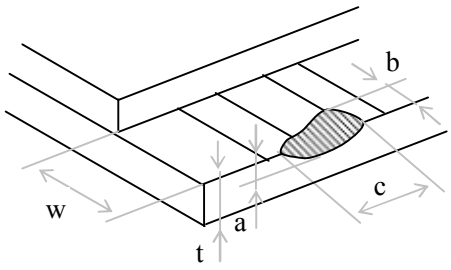
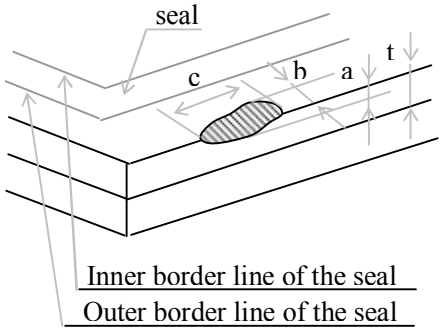
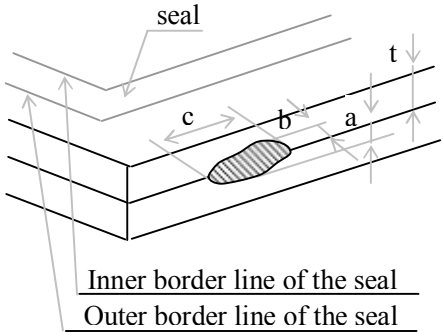
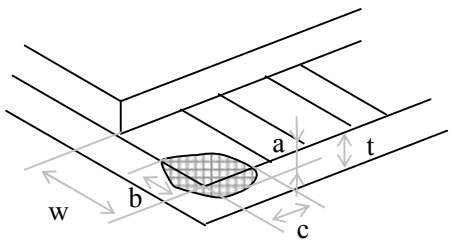
| Outgoing Inspection standard | Inspection conditions | Inspection | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Unit | IL | AQL |
| Major Defects | See 8.3 general notes | See 8.5 | | | II | 0.065 |
| Minor Defects | See 8.3 general notes | See 8.5 | | | II | 0.065 |
| Note：Sampling standard conforms to GB2828 | | | | | | |

## 9.5 Inspection Items and Criteria

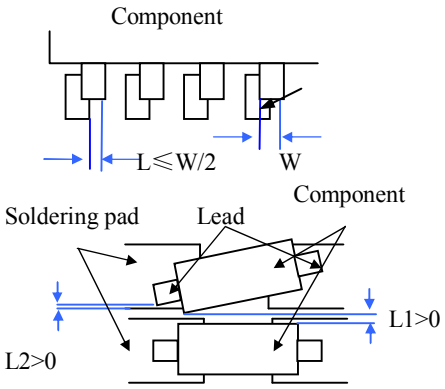
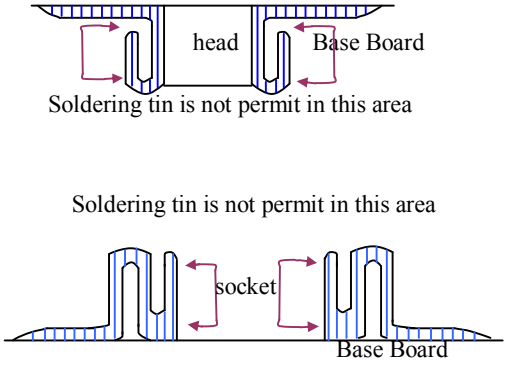
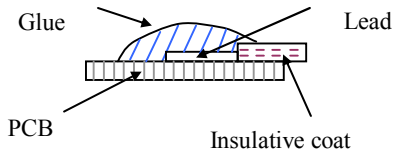
| Inspection items | | | Judgment standard | | | |
|---|---|---|---|---|---|---|
| | | | Category | | Acceptable number | |
| | | | | | A zone | B zone |
| 1 | Black spot, White spot, Pinhole, Foreign Particle, Particle in or on glass, Scratch on glass |  (a/b<2.5) | A | Φ<=0.20 | Neglected | Neglected |
| | | | B | 0.20<Φ<=0.25 | 3 | Neglected |
| | | | C | 0.25<Φ<=0.3 | 2 | Neglected |
| | | | D | 0.3<Φ<=0.4 | 1 | 3 |
| | | | E | 0.4<Φ<=0.5 | 0 | 2 |
| | | | Total defective point(B,C) | | 1 | - |
| 2 | Black line, White line, and Particle Between Polarizer and glass, Scratch on glass |  L/W>=2.5 | A | W<=0.03 | Neglected | Neglected |
| | | | B | 0.03<W<=0.05<br>L<=3.0 | 3 | Neglected |
| | | | C | 0.05<W<=0.1<br>L<=3.0 | 2 | Neglected |
| | | | D | 0.05<W<=0.1<br>L<=4.0 | 1 | 3 |
| | | | E | W>0.1<br>L>4.0 | 0 | 2 |
| | | | Total defective point(B,C) | | 1 | - |
| 3 | Bright spot | | any size | | none | none |
| 4 | Contrast variation |  | A | Φ<0.2 | Neglected | Neglected |
| | | | B | 0.2<Φ<=0.3 | 2 | |
| | | | C | 0.3<Φ<=0.4 | 1 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | D | 0.4<Φ | 0 | |
| | | | Total defective point(B,C) | | 3 | |
| 5 | Bubble inside cell | | any size | | none | none |
| 6 | Polarizer defect (if Polarizer is used) | Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass. | Refer to item 1 and item 2. | | | |
| | | Bubble, dent and convex | A | Φ<=0.1 | Neglected | Neglected |
| | | | B | 0.1 <Φ<=0.2 | 2 | Neglected |
| | | | C | 0.2 <Φ<=0.3 | 1 | 2 |
| 7 | Surplus glass | Stage surplus glass  | B<=0.3mm | | | |
| | | Surrounding surplus glass  | Should not influence outline dimension and assembling. | | | |
| 8 | Open segment or open common | | Not permitted | | | |
| 9 | Short circuit | | Not permitted | | | |
| 10 | False viewing direction | | Not permitted | | | |
| 11 | Contrast ratio uneven | | According to the limit specimen | | | |
| 12 | Crosstalk | | According to the limit specimen | | | |
| 13 | Black /White spot(display) | | Refer to item 1 | | | |
| 14 | Black /White line(display) | | Refer to item 2 | | | |

| Inspection items | Judgment standard |
|---|---|

| | | | Category(application: B zone) | | Acceptable number |
|---|---|---|---|---|---|
| 15 | Glass defect crack | ⅰ) The front of lead terminals<br>  | A | a≤ t, b≤1/5W, c≤3mm | Max.3 defects allowed |
| | | | B | Crack at two sides of lead terminals should not cover patterns and alignment mark | |
| | | ⅱ) Surrounding crack-non-contact side<br>  | b < Inner borderline of the seal | | |
| | | ⅲ) Surrounding crack- contact side<br>  | b < Outer borderline of the seal | | |
| | | ⅳ) Corner<br>  | A | a <= t, b <= 3.0, c <= 3.0 | |
| | | | B | Glass crack should not cover patterns u and alignment mark and patterns. | |

| Inspection items | Judgment standard |
|---|---|

| | | | Category(application: B zone) |
|---|---|---|---|
| 16 | PCB defect | Component soldering:<br>No cold soldering、short、open circuit、burr、tin ball<br>The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1)；<br>the sheet component deviation:<br>Pin deviates from the pad and contact with the near components is not permitted（Pic.2） |  |
| | | lead defect:<br>The lead lack must be less than 1/3 of its width;<br>The lead burr must be less than 1/3 of the seam;<br>Impurities connect with the near leads is not permitted | |
| | | Connector soldering:<br>Soldering tin is at contact position of the plug and socket is not permitted<br>No foundation is scald<br>Serious cave distortion on plug and socket contact pin is not permitted |  |
| | | Glue on root of the speaker receiver and motor lead:<br>The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat. |  |

# 10. Precautions for Use of LCD Modules

## 10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct

assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

**10.2 Storage precautions**

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

**10.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.**